800 Gb/s DR8 OSFP 500 m Optical Transceiver

OSFP Series

- OSFP form factor hot pluggable
- CMIS compliance
- 8 channels of 100G-PAM4 electrical and optical parallel lanes
- Single optical port of MPO-16/APC
- Top closed fin
- 500m maximum reach via single mode fiber
- 16 Watts max
- Case temperature range of 0°C to 70°C

Ascent's OSFP-800G-DR8-05 is an 800 Gb/s Octal Small Form-factor Pluggable (OSFP) optical module with top closed fin designed for 500m optical communication applications.

The module converts 8 channels of 100 Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100 Gb/s operation for an aggregate data rate of 800 Gb/s.

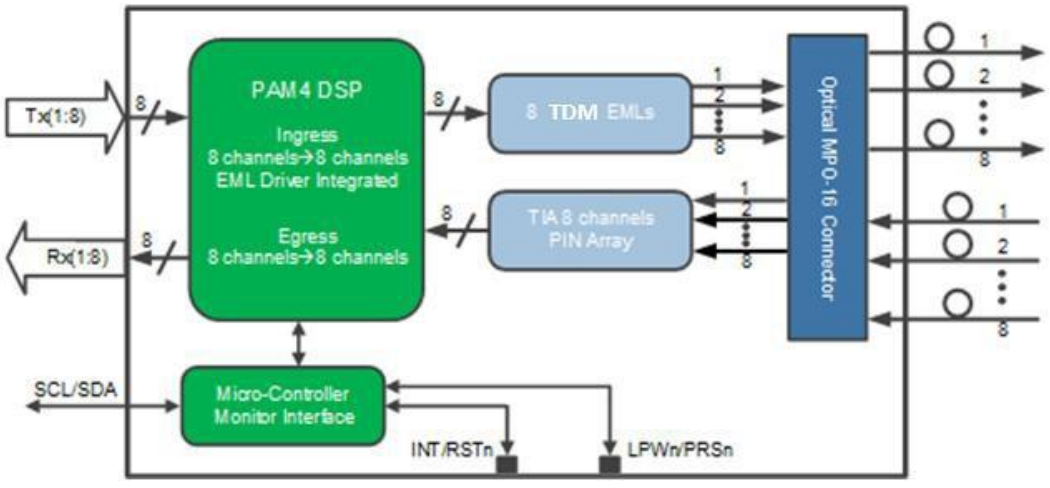
An optical fiber cable with an APC/MPO-16 connector can be plugged into the OSFP112 DR8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector. I2C interface is supported to read and control the status of this product.

This transceiver is compliant with lEEE P802.3ck, IEEE 802.3cu, OSFP MSA. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Data Center, Breakout 2x 400G DR4 or 8x 100G DR Application.

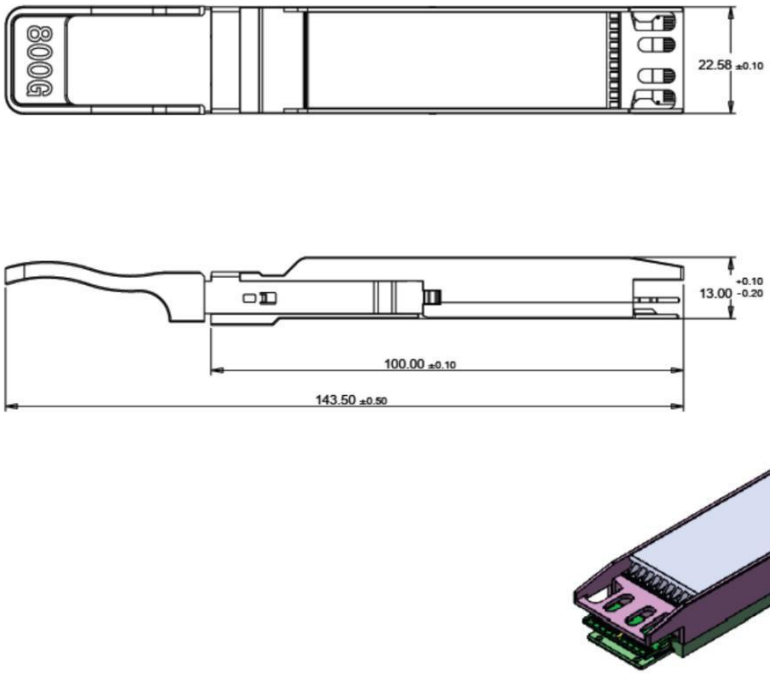
Key Features

- Common Management Interface Specifications (CMIS)
- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

Transceiver Block Diagram



Mechanical Diagram

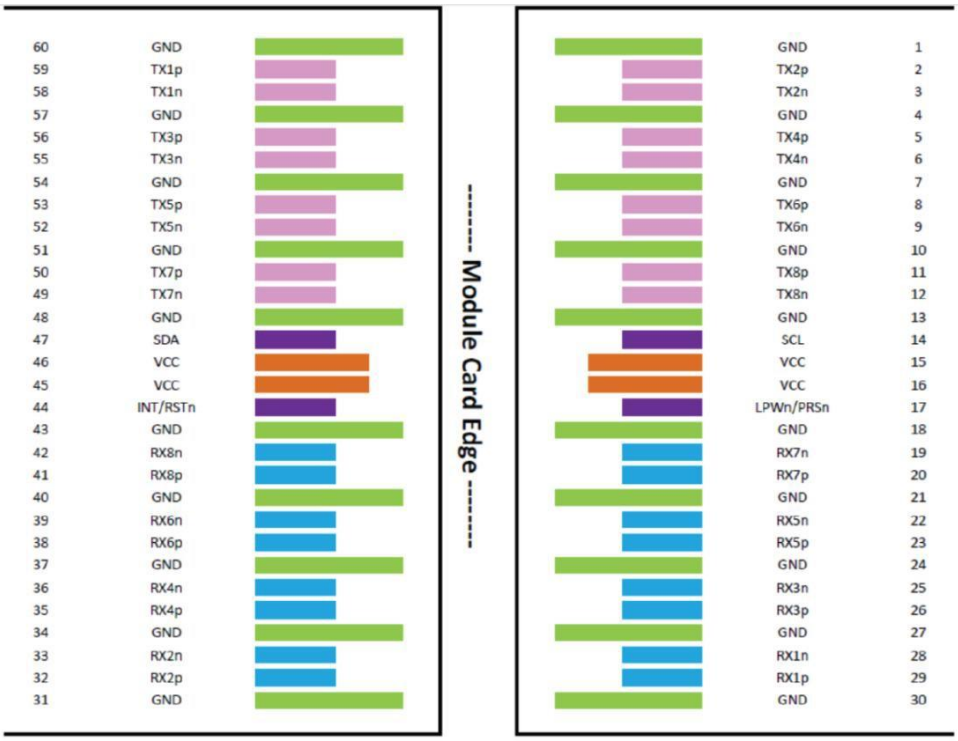


CMIS Application Advertisements

ApSel Code	Host Electrical Interface	Module Media Interface	Host and Media Lane Count	Host Lane Assignment
ApSel 1	50 (400GAUI-4-L C2M)	1C (400GBASE-DR4)	44 (4:4)	11 (lanes 1, 5)
ApSel 2	32 (IB NDR)	1C (400GBASE-DR4)	44 (4:4)	11 (lanes 1, 5)
ApSel 3	F (200GAUI-4 C2M)	17 (200GBASE-DR4)	44 (4:4)	11 (lanes 1, 5)
ApSel 4	31 (IB HDR)	17 (200GBASE-DR4)	44 (4:4)	11 (lanes 1, 5)
ApSel 5	4C (100GAUI-1-L C2M)	14 (100GBASE-DR)	11 (1:1)	FF (lanes 1, 2, 3, 4, 5, 6, 7, 8)
ApSel 6	52 (800GAUI-8-L C2M)	0 (Undefined)	88 (8:8)	01 (lane 1)
ApSel 7	4F (400GAUI-4-S C2M)	1C (400GBASE-DR4)	44 (4:4)	11 (lanes 1, 5)
ApSel 8	4B (100GAUI-1-S C2M)	14 (100GBASE-DR)	11 (1:1)	FF (lanes 1, 2, 3, 4, 5, 6, 7, 8)
ApSel 9	51 (800GAUI-8-S C2M)	0 (Undefined)	88 (8:8)	01 (lane 1)
ApSel 10	42 (CAUI-4 C2M with RS FEC)	F (100G PSM4 MSA)	44 (4:4)	11 (lanes 1, 5)
ApSel 11	30 (IB EDR)	F (100G PSM4 MSA)	44 (4:4)	11 (lanes 1, 5)

Pin Assignment

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in the figure below, which is defined in Clause 8.1 of OSFP MSA Specification.



MSA Compliant Connector

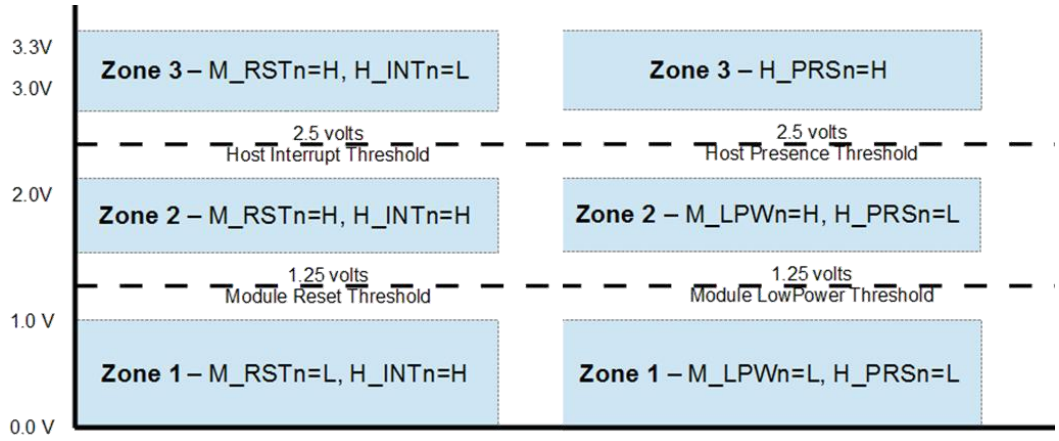
Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2

17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

OSFP Control Pins

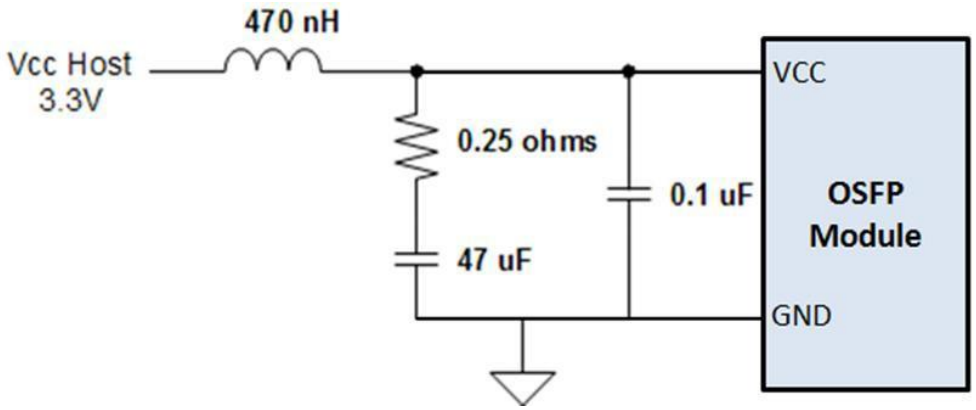
Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Input/Output	Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3.
INT/RSTn	Input/Output	Dual Function Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3.

Voltage Zones



Voltage Zones

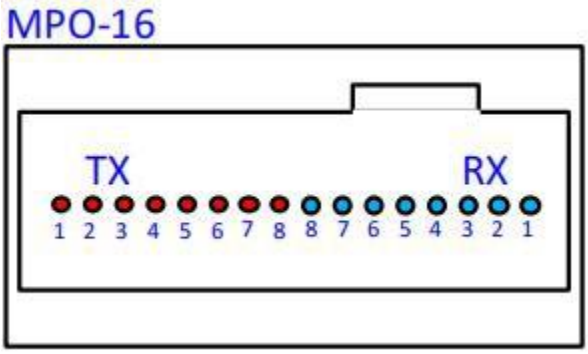
Recommended Power Supply Filter



Optical Port Description

The optical interface port is an MPO-16 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with

the connector keyway feature on top.



Optical Media Dependent Interface Port Assignments

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Specifications

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-40	85	°C	
Operating Case Temperature	T_{OP}	0	70	°C	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity	RH	0	85	%	Non-condensing

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-15}$		1
Link Distance	D	2		500	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min.	Typ.	Max.	Units	Note
Power Consumption				16	W	
Supply Current	I_{CC}			4.84	A	
Module Input (each Lane)						
Signaling Rate, each Lane	TP1	53.125 ppm ± 100 ppm			GBd	
DC Common-Mode Input Voltage	TP1	-0.35		2.85	V	
Single-Ended Input Voltage	TP1a	-0.4		3.3	V	
AC Common-Mode Voltage Tolerance	TP1a				mV	
Low-Frequency, VCM_{LF}		32				
Full-Band, VCM_{LF}		80				
Module Stressed Input Tolerance	TP1a	IEEE 802.3ck D3.3 120G.3.4.3				
Differential Peak-to-Peak Input Voltage Tolerance	TP1a	750			mV	
Differential to Common-Mode Return Loss, RLcd	TP1	IEEE 802.3ck D3.3 Equation 120G-2			dB	
Effective Return Loss, ERL	TP1	8.5			dB	
Differential Termination Mismatch	TP1			10	%	

Signaling Rate, Each Lane	TP4	53.125 ± 100 ppm		GBd
Peak-to-Peak AC Common-Mode Voltage	TP4			mV
Low-Frequency, VCM_{LF}			32	
Full-Band, VCM_{LF}			80	
Differential Peak-To-Peak Output Voltage	TP4			mV
Short Mode			600	
Long Mode			845	
Eye Height	TP4	15		mV
Vertical Eye Closure, VEC	TP4		12	dB
Common-Mode to Differential Return Loss, Rldc	TP4	IEEE 802.3ck Equation 120G-1		dB
Effective Return Loss, ERL	TP4	8.5		dB
Differential Termination Mismatch	TP4		10	%
Transition Time	TP4	8.5		ps
DC Common-Mode Voltage Tolerance	TP4	-0.35	2.85	V

Optical Characteristics

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Note**
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	P_{AVG}	-2.9		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-0.8		4.2	dBm	2
Launch Power in OMA_{outer} minus TDECQ						
For ER ≥ 5 dB		-2.2			dB	
For ER < 5 dB		-1.9			dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
TDECQ – $10log_{10}(C_{eq})$				3.4	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time				17	ps	
$RIN_{15.5}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			15.5	dB	
Transmitter Reflectance	R_T			-26	dB	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				

Damage Threshold, each Lane	THd	5			dBm	3
Average Receive Power, each Lane		-5.9		4	dBm	4
Receive Power (OMA_{outer}), each Lane				4.2	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			Equation (1)	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-1.9	dBm	6
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-15		-9.9	dBm	
LOS De-assert	LOSD			-6.9	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
SECQ - $10\log_{10}(C_{eq})$				3.4	dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. The values for OMA_{outer}(min) vary with TDECQ. The figure below illustrates this along with the values for OMA_{outer}(max).

3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5. Receiver sensitivity (OMAouter) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in the figure below.

Equation (1): RS = max(-3.0, SECQ - 5.3) dBm

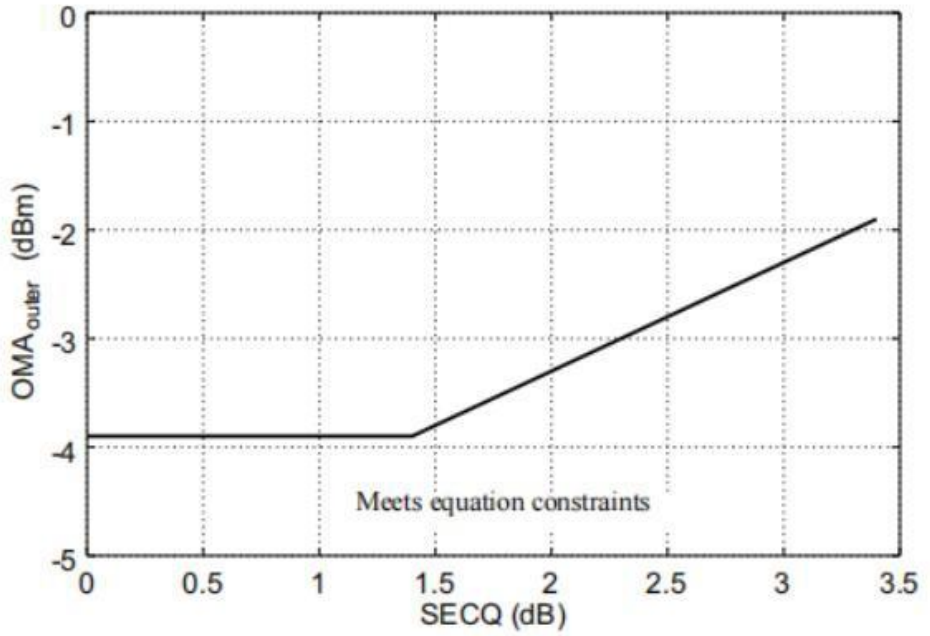
RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

6. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.

7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristic of the receiver.

Illustration of Receiver Sensitivity



Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional ±1 dB fluctuation, or a ±3 dB total accuracy.

Ordering Information

Product Name	Product Description
OSFP-800G-DR8-05	800GBASE-DR8 OSFP PAM4 1310 nm 500 m DOM MTP/MPO-16 SMF Optical Transceiver Module

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Specifications and product availability are subject to change without notice.

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