100 Gb/s 120km QSFP28 Coherent Transceiver

QSFP28 Series



- **Hot-pluggable**
- **Transmission reaches up to 120km in unamplified applications**
- **Duplex LC connector**
- **Metal package for lower EMI**
- **Single 3.3V power supply**
- **Maximum power consuconsumption 13W(ST), 15W(IT)**
- **RoHS-6 compliant**

Ascent's 100G Coherent is a 100Gbps QSFP28 optical module designed for single or multi-span DWDM links, as well as unamplified point-to-point links up to 120km. The module allows for dispersion compensation of standard single-mode fiber up to a distance of 2,000km depending on FEC mode.

The product is designed with form factor and optical/electrical connection according to the QSFP28 MSA with DD and the Common Management Interface Specification (CMIS) in the OIF Coherent CMIS implementation agreement.

Key Features

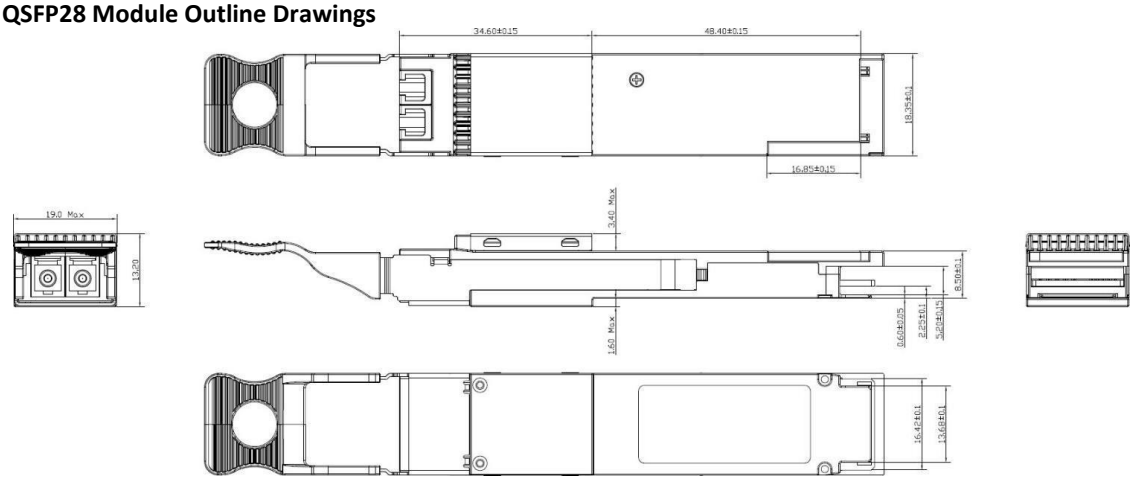
- Digital Coherent Optics module, QSFP28 form factor, (DD)
- Option for leveraging legacy QSFP28 slots
- Support full 100GE and OTU4 host client interfaces and framer monitoring functions
- DP-(d)QPSK modulation
- Hot pluggable
- Transmission reaches up to 120km in unamplified applications
- Full C-band tunable, grid-less
- Duplex LC connector
- Metal package for lower EMI
- Single power supply voltage: +3.3V
- Operating Case Temperature

  ST: -5°C to +70°C

  IT: -40°C to +85°C
- Maximum power consumption: 13W(ST), 15W(IT)
- RoHS6 Compliant

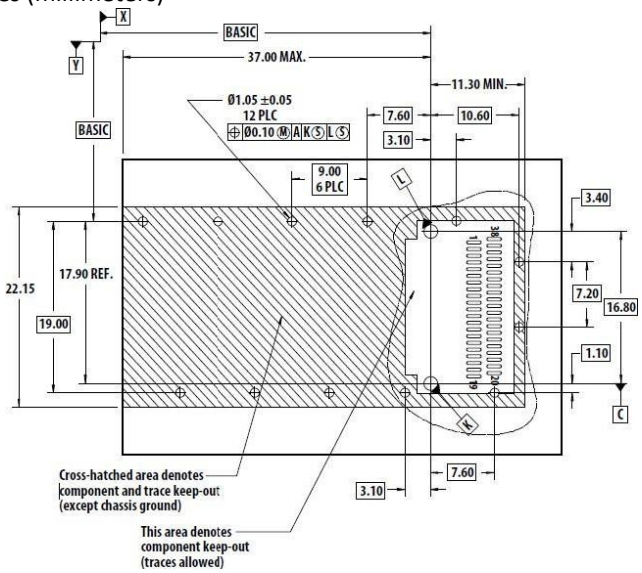
Outline Diagram

QSFP28 Module Outline Drawings



QSFP28 Host Board Mechanical Footprint

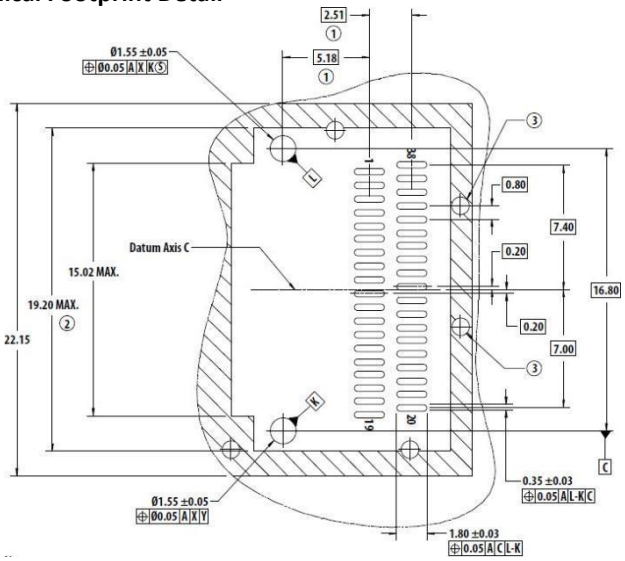
Dimensions are in inches (millimeters)



Notes:

1. Datum X & Y are established by the customer's fiducial.
2. Datum A is the top surface of the host board.
3. Location of the edge of PCB is application specific.
4. Finished hole size.

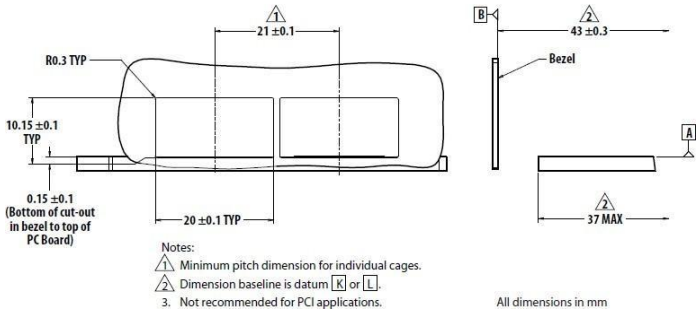
QSFP28 Host Board Mechanical Footprint Detail



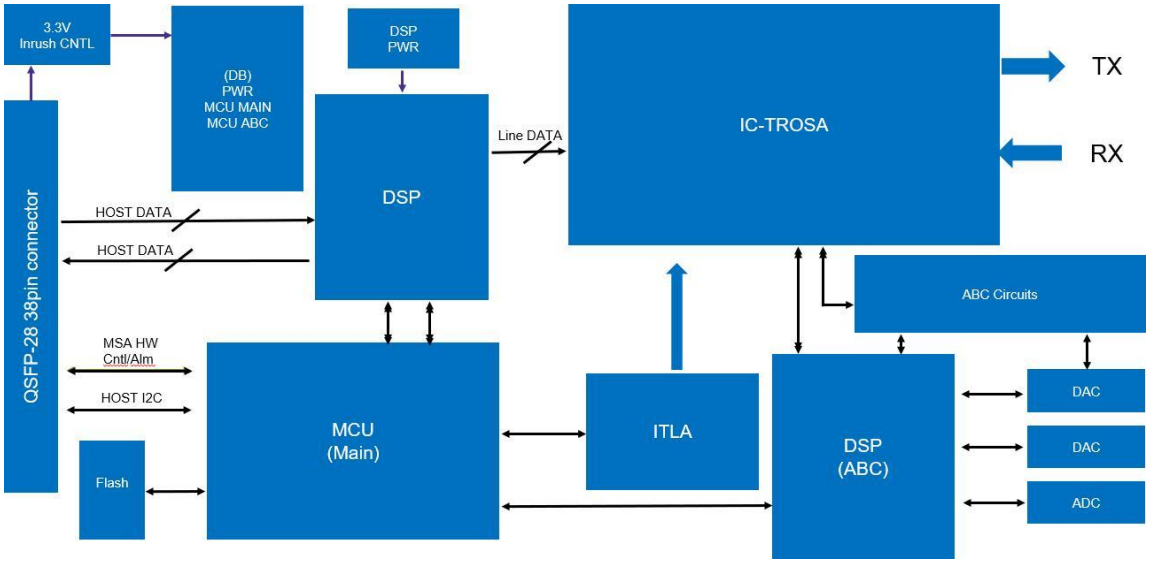
Notes:

1. Center.
2. Surface traces permitted within this length.
3. Indicated holes are optional

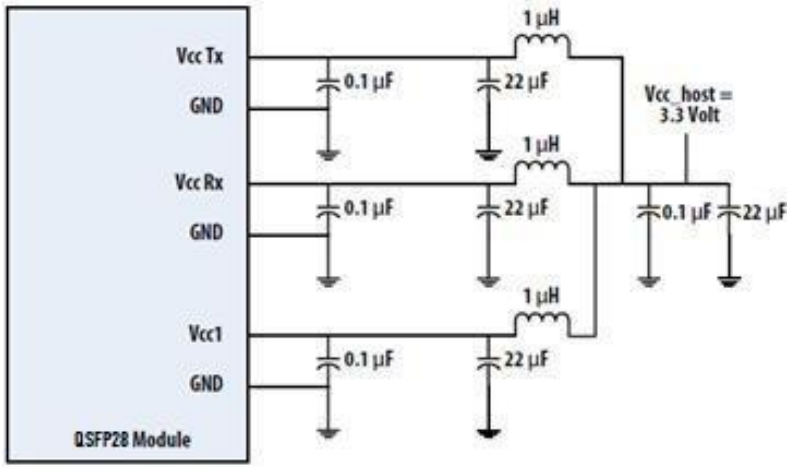
Host Board Bezel Design



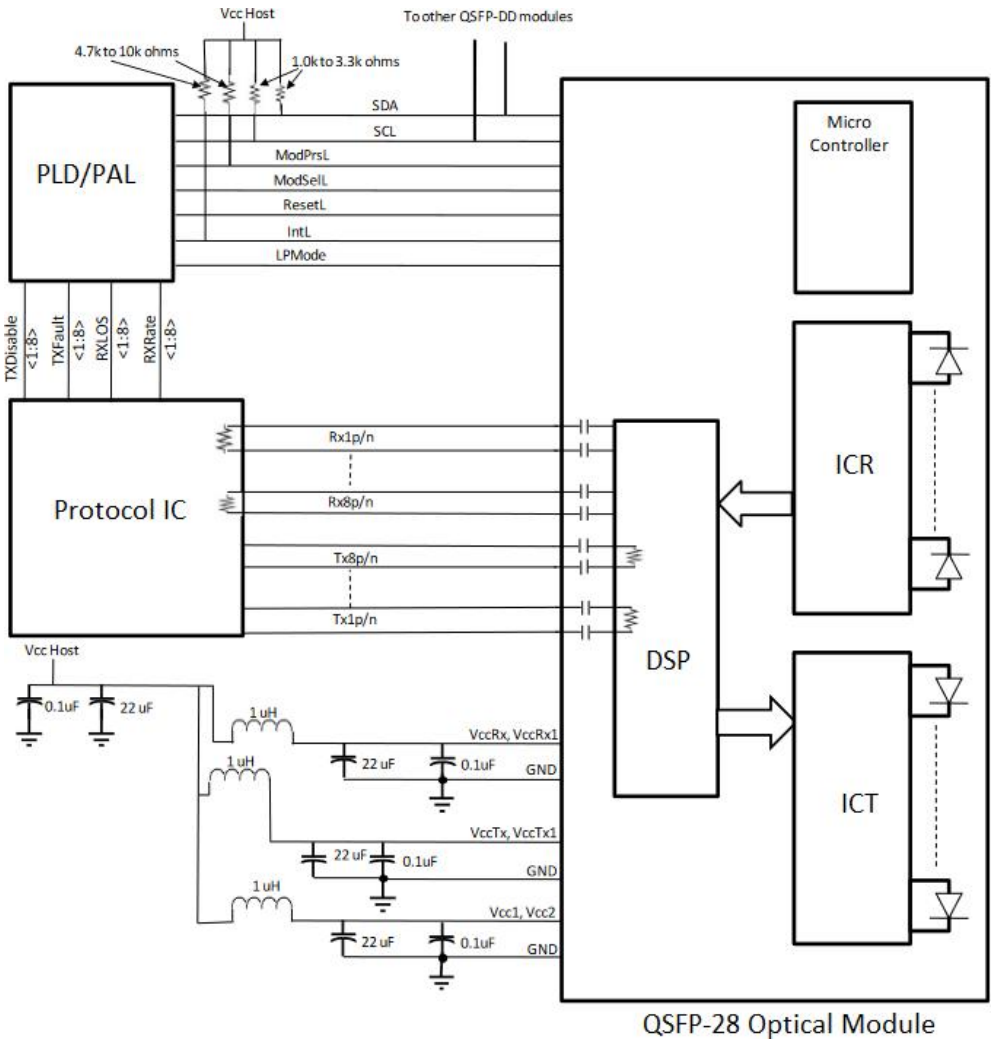
QSFP28 DCO Module Functional Block Diagram



Recommended Host Board Supply Filtering Network



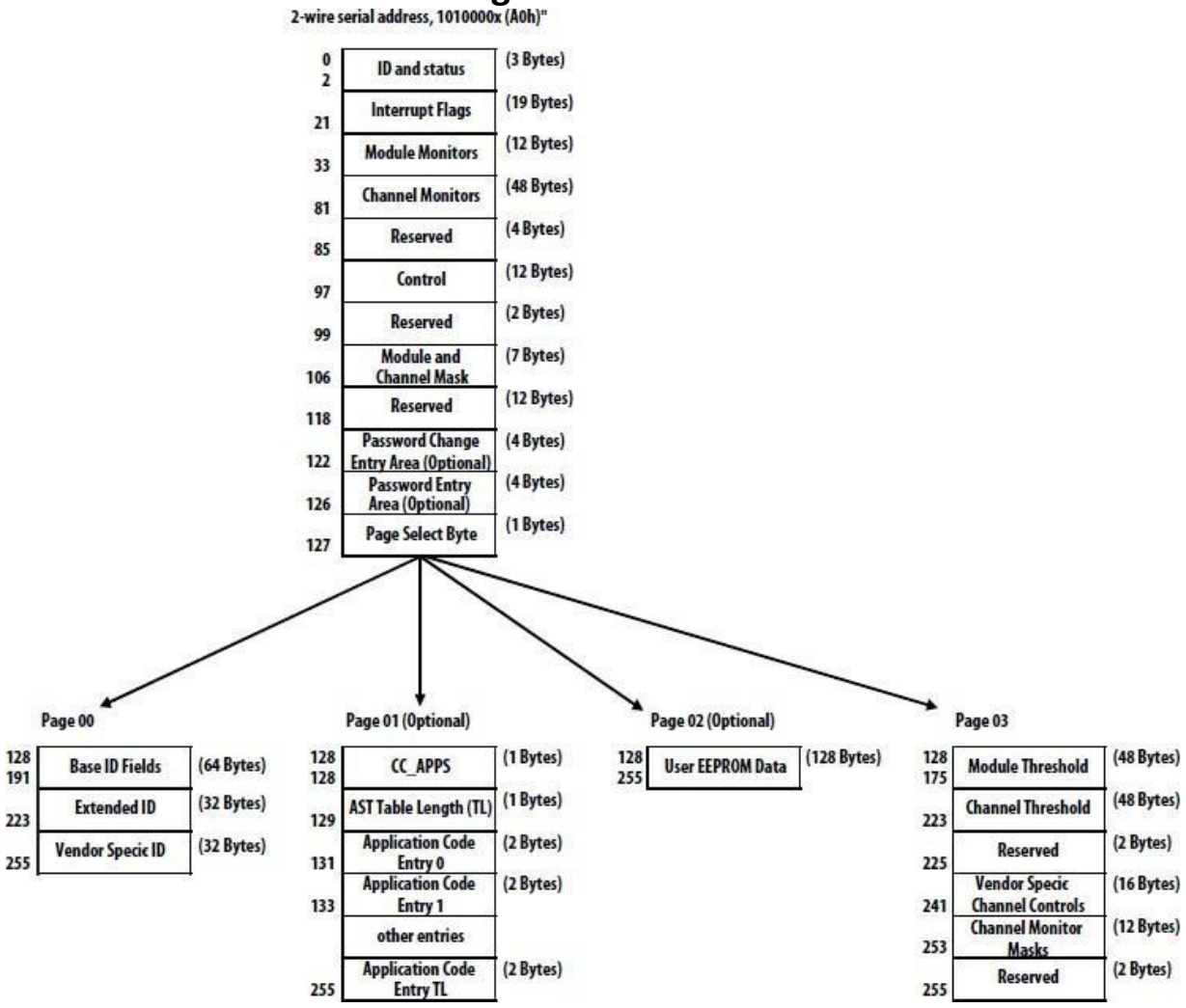
QSFP-28 Host Board Schematic



Digital Diagnostic Monitoring and Serial ID Operation

The memory is structured as a single address, multiple page approach. The address is given as A0h. The structure of the memory is shown in section 8.1. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages of 128bytes each. This structure permits timely access to addresses in the lower page, e.g., Interrupt Flags and Monitors. Less time critical entries, e.g., serial ID information and threshold settingsare available with the Page Select function. The information stored in the EEPROM, including the organization and the digital diagnostic information, is defined in SFF-8636, Specification for Management Interface for 4-lane Modules and Cables, Rev 2.10a (September 24, 2019). For details, refer to Application Note 100G QSFP28 Coherent EEPROM MapRev_A.1, 15-Nov-2021.

Two-Wire Serial Address A0h Page Structure

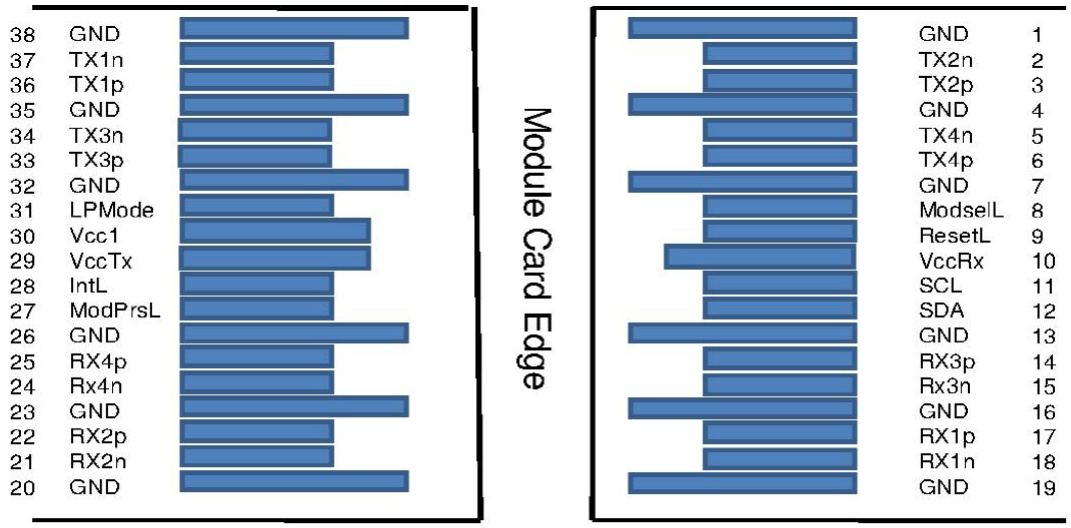


Diagnostics

The enhanced digital diagnostics feature monitors five key transceiver parameters which are internally calibrated and should be read as absolute values.

Address	Parameter	Range	Accuracy	Unit
Lower Page 00h, 22-23	Temperature	-5 to 70	+/- 3°C	°C
Lower Page 00h, 26-27	V_{CC}	3.13 to 3.47	+/- 3V	V
Lower Page 00h, 50-51	Tx Output Power	-3 to -10	+/- 2dB	dBm
Lower Page 00h, 42-43	Tx Bias Current	40 to 130	+/- 3%	mA
Lower Page 00h, 34-35	Rx Input Power	0 to -20	+/- 1dB	dBm
		-21 to -29	+/-2dB	dBm
		< -30	+/-3dB	dBm

Pin Assignment



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin	Logic	Symbol	Description	Plug Seq.*	Note
1	-	GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4	-	GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7	-	GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10	-	Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13	-	GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16	-	GND	Ground	1	1
17	CML-O	Rx1n	Receiver Inverted Data Output	3	
18	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
19	-	GND	Ground	1	1
20	-	GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23	-	GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26	-	GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	

Pin	Logic	Symbol	Description	Plug Seq.*	Note
29	-	Vcc Tx	+3.3V Power Supply Transmitter	2	2
30	-	Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32	-	GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35	-	GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38	-	GND	Ground	1	1

*Plug Seq.: Pin engagement sequence during hot plugging.

Note：

1. GND is the symbol for signal and supply(power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal- common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 5-6 of SFF-8679. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Specifications

General Operating Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Absolute Supply Voltage	Vcc_max	0	-	4.0	V	-
Operating Voltage	Vcc	3.135	-	3.465	V	-
Power Consumption	-	-	-	13	W	1
	-	-	-	15	W	
Operating Case Temperature (ST)	Top	-5	-	70	°C	2
Operating Case Temperature (IT)	Top	-40		85	°C	-
Storage and Transportation Temperature	Tst	-40	-	85	°C	4
Relative Humidity	RH	5	-	85	100%	3
Maximum Transmission Distance (unamplified)	Dmax	-	-	120	km	-

Note:

1. For SCFEC, Other modes incl. SDFEC are TBD. 13W for ST and 15W for IT.
2. Measured on top side front center of QSFP28 module.
3. Non-condensing.

Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Symbol Rate	Gbaud	-	-	32	GBd	-
Modulation Format	-		DP-(d)QPSK		-	-
Channel Frequency Range	-	191.3	-	196.1	THz	
Channel Spacing	-	-	50	-	GHz	2
Frequency Accuracy	-	-2.5	-	2.5	GHz	-
Laser Intrinsic Linewidth	LW	-	-	300	KHz	4
Relative Intensity Noise	-	-	-	-140	dB/Hz	-

Note:

Transmitter Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Data rate	-	-	-	128	Gb/s	-
Side Mode Suppression Ratio	SMSR	40	-	-	dB	-
Tx Output Power	Pt	-8	-	-5	dBm	-
Tx Output Power Monitor Accuracy	-	-2	-	2	dB	-
Tx Output Power Imbalance Between X-Pol and Y-Pol	Px/y	-	-	2	dB	-
Tx XY Skew	LW	-	-	3	ps	-
Tx IQ Offset	-	-	-	-24	dB	-
Tx IQ Imbalance	-	-	-	1	dB	-
Tx Quadrature Error	-	-5	-	5	degree	-
Tx IQ Skew	-	-	-	2	ps	-
Tx Error Vector Magnitude Mask Ratio	EVM	-	-	18	%	-
Tx In-Band OSNR	OSNRin	40	-	-	dB/0.1nm	-
Parameter	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**	**Note**

Tx Reflectance	-	-	-	-22	dB	-

Receiver Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Rx Signal Input Power (Unamplified)	Pin	-40	-	+5	dBm	-
Average Rx Sensitivity	Rsen	-	-	-32	dBm	-
CD Tolerance	-	-	-	10	ns/nm	1
PMD Tolerance	-	-	-	16	ps	2
Polarization Dependent Loss(2dB) OSNR Penalty	-	-	-	1	dB	-
Rx Signal Input Power Transient Amplitude	-	-3	-	3	dB	-
State of Polarization Tracking (< 0.5dB OSNR Penalty)		-	-	100	KHz	
Rx Signal Input Power Transient Rise/Fall Time	-	0.1	-		ms	-
Rx Signal Input Power Monitor Range	-	-40	-	+5	dBm	-
Rx Signal Input Power Monitor Accuracy	-	-3	-	3	dB	-
Rx Reflectance	-	-	-	-22	dB	-
LOS Assert	LOS A	-40	-	-	dBm	-
LOS De-assert	LOS De	-	-	-32	dBm	-
LOS Hysteresis	-	0.5	-	5	dB	-
Metro OSNR	OSNRmin	16.5	-	-	dB/0.1nm	3
	OSNRmin	15	-	-	dB/0.1nm	4
LH OSNR	OSNRmin	11.2	-	-	dB/0.1nm	5
	OSNRmin	11	-	-	dB/0.1nm	6

Notes:

1. For SCFEC. Other modes with higher CD tolerance incl. SDFEC are TBD.
2. First and second order PMD to the Maximum Mean DGD.
3. DQPSK, GFEC 7% OH, 28Gbaud, dispersion tolerance up to 100km on SMF.
4. DQPSK, SCFEC 7% OH, 28Gbaud, dispersion tolerance up to 500km on SMF.
5. QPSK, OFEC 15% OH, 31.57Gbaud, dispersion tolerance up to 2,000km on SMF, will be supported in the near future.
6. QPSK, OFEC 15% OH, 30Gbaud, dispersion tolerance up to 2,000km on SMF, will be supported in the near future Laser Safety: All transceivers in this datasheet are Class I Laser products per FDA/CDRH and IEC-60825 standards. They must be operated under specified operating conditions.

Electrical Characteristics (Over Operating Case Temperature Range, Vcc = 3.14V to 3.47V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Data Rate, NRZ	-	25.8	-	27.9	Gb/s	-
Differential pk-pk Input Voltage	-	900	-	-	mVpp	-
DifferentialTermination Mismatch	-	-	-	10	%	-
Differential Input Return Loss	-	CEI-28G VSRTP1 SDD11			dB	-
Parameter	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**	**Note**

Differential to Common Mode Input Return Loss	-	CEI-28G VSRTP1 SDC11			dB	-
Module Stressed Input Test	-	SeeOIFCEI-03.1			-	-
Receiver						
Data Rate, NRZ	-	25.8	-	27.9	Gb/s	-
Differential Pk-Pk Output Voltage	-	750	-	900	mVpp	-
AC Common Mode Output Voltage, RMS	-	-	-	17.5	mV	-
Differential Termination Mismatch	-	-	-	10	%	-
Differential Output Return Loss	-	CEI-28G VSR TP4	dB	-		
Common to Diff. Mode Conversion Return Loss	-	CEI-28G VSR TP4 SDC22	dB	-		
Transition Time, 20% to 80%	-	12	-	-	ps	-
Eye Width @1E-15 Probability (EW15)	-	0.57	-	-	UI	-
Eye Height @1E-15 Probability (EH15)	-	228	-	-	mV	-
Common Mode Return Loss (250MHz to 30GHz)	-	-	-	-2	dB	-
Vertical Eye Closure	-	-	-	5.5	dB	-

Timing of Control and Status

Parameter	Min	Typ.	Max	Unit	Conditions
Mgmtinit Duration			2000	ms	Time from power on1, hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction
Reset Assert Time		5		us	Minimum pulse time on the ResetL signal to initiate a module reset
Int/RxLOS Mode Change			100	ms	Time to change between IntL and RxLOSL modes of the dual- mode signal IntL/RxLOSL
LPMode/TxDis Mode Change Time			100	ms	Time to change between LPMode and TxDis modes of LPMode/TxDis
IntL Assert Time		40		ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time			500	us	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
Rx LOS Assert Time		40		ms	Time from Rx LOS state to Rx LOS bit set(value = 1b) and IntL asserted
TX Disable Assert Time			150	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal
TX Disable Deassert Time			300	ms	Time from Tx Disable bit cleared to 1 until optical output rises above 90% of nominal
Tx Fault Assert Time			200	ms	Time from Tx Fault state to Tx Fault bit set(value=1b) and IntL asserted

Ordering Information

Product Name	Product Description
Q28-100GDCO-ZRLP	Coherent 100G ZR QSFP28 transceiver module, Full C-band tunable, grid-less , Duplex LC connector

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