40 Gb/s 150m MTP/MPO QSFP+ SR4 Transceiver with DDM

QSFP+ Series

- **Compliant with SFF-8436**
- **Compliant with IEEE 802.3 40GBASE-SR4**
- **Maximum link length of 100m on OM3 MMF or 150m on OM4 MMF**
- **Max. Power < 1.5W**
- **2-wire interface for management and DDM**

Ascent's QSFP+ transceiver modules are designed for use in 40 Gigabit per second links over multimode fiber. They are compliant with the SFF-8436 and IEEE 802.3 40GBASE-SR4. Digital diagnostics functions are available via a I^2C interface, including Tx and Rx power monitoring. The optical transceiver is compliant per the RoHS Directive 2011/65/EU.

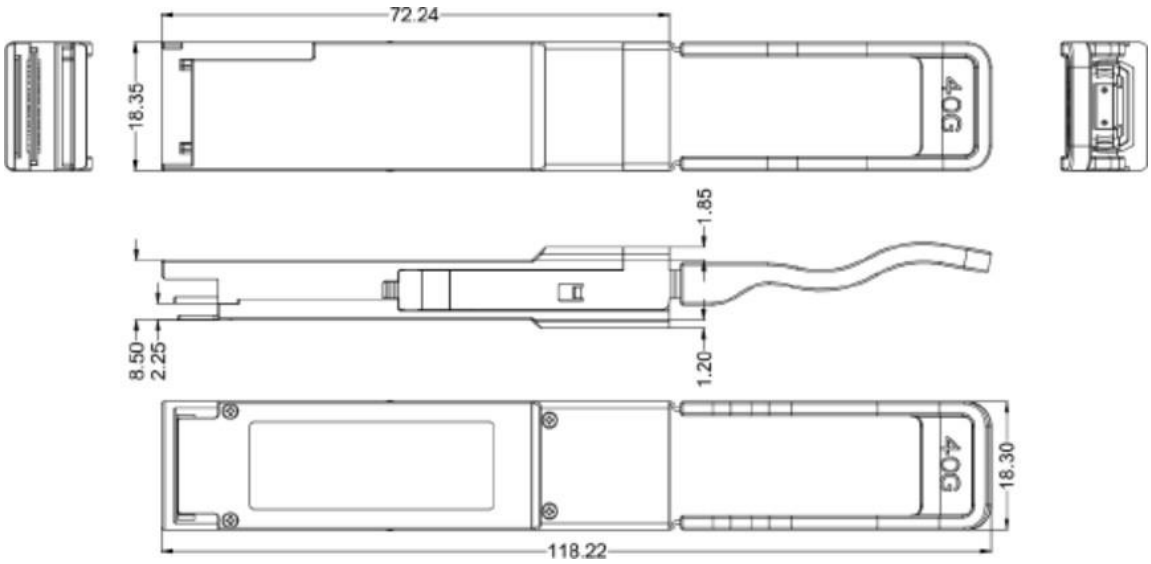
The optical transmitter portion of the transceiver incorporates a 4-channel VCSEL array, a 4-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. For module control, the control interface incorporates a Two Wire Serial interface of clock and data signals. Diagnostic monitors for VCSEL bias, module temperature, transmitted optical power, received optical power and supply voltage are implemented and results are available through the TWS interface. Alarm and warning thresholds are established for the monitored attributes. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm/warning and fault information are available via the TWS interface.

The optical receiver portion of the transceiver incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, a 4-channel output buffer, diagnostic monitors, and control and bias blocks. Diagnostic monitors for optical input power are implemented and results are available through the TWS interface. Alarm and warning thresholds are established for the monitored attributes.

Key Features

- Compliant with SFF-8436
- Compliant with IEEE 802.3 40GBASE-SR4
- 850nm 4 VCSEL Lasers and 4 channels PIN photo detectors
- Maximum link length of 100m on OM3 MMF or 150m on OM4 MMF
- 3.3V Supply Voltage
- Max. Power <1.5W
- 0-70°C Case Operating Temperature
- MPO Receptacle
- Maximum Data Rate per Lane: 10.3125Gb/s
- 2-wire interface for management and DDM
- Complies with EU Directive 2011/65/EU
- Class 1 Laser

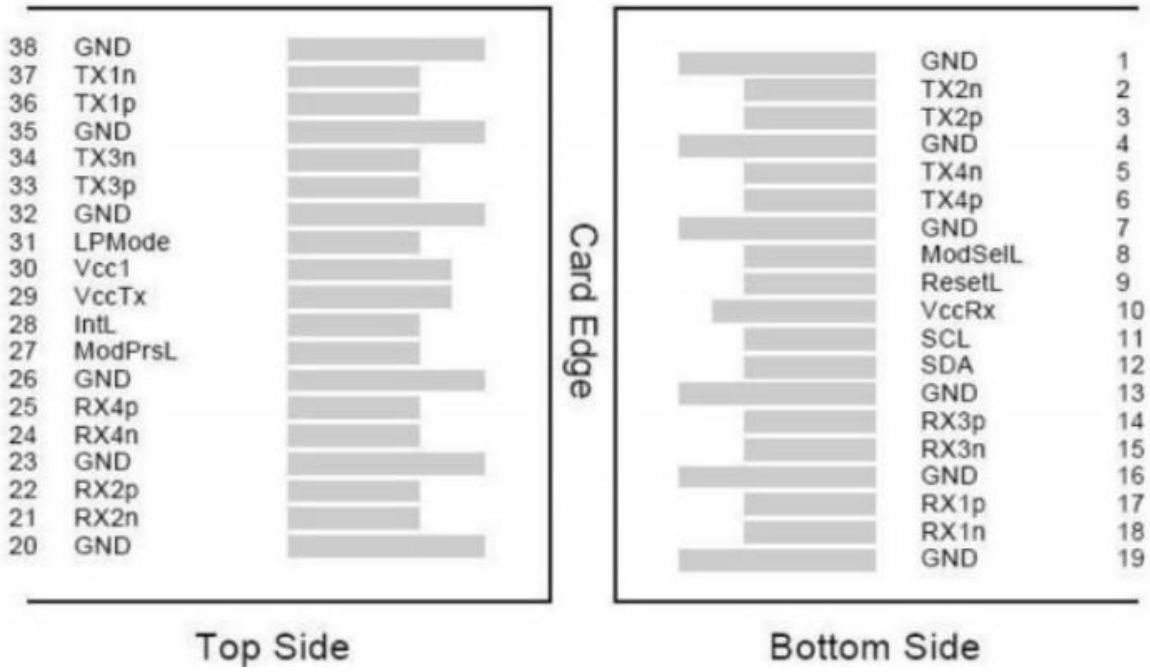
Outline Diagram



Digital Diagnostics Function

Parameter	Symbol	Min	Typ.	Max
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V_{CC}	±3	%	Internal
Tx Bias Current (Each Lane)	0 to 15	±10	%	Internal
Tx power (Each Lane)	-7.6 to 2.4	±3	dB	Internal
Rx Power (Each Lane)	-9.5 to 2.4	±3	dB	Internal

Pin Assignment



Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire serial Interface Data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	

Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power Supply Transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3n	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3p	Transmitter Inverted Data Output	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Storage Temperature	Ts	-40	-	+85	°C	
Relative Humidity (non-condensing)	RH	5	-	95	%	
Supply Voltage	Vcc	-0.5	-	3.6	V	
Input Voltage	Vin	-0.5	-	Vcc+0.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Operating Case Temperature	T_{OPR}	0	-	70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Supply Current	Icc			475	mA	
Maximum Power Consumption	P_D	-	-	1.5	W	
Data Rate per Lane	DR	-	10.3125	-	Gb/s	
Operating Distance (MMF OM3)	-	0.5	-	100	m	
Operating Distance (MMF OM5)	-	0.5	-	150	m	

Optical and Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Mean Wavelength (Each Lane)	λ	840	850	860	nm	
Data Rate per Lane	DR		10.3125		Gbps	
Spectral Width (RMS)	Δλ			0.65	nm	
Optical Power (Each Lane)	P_{OUT}	-7.6	-	2.4	dBm	
OMA per Lane	P_{oma}	-5.6		3	dBm	
Peak Power, each Lane	P_peak			4	dBm	
Extinction Ratio	ER	3			dB	
TDP, each Lane	TDP			3.5	dB	
Optical Return Loss Tolerance				12	dB	
Average Launch Power Tx_Off(Each Lane)				-30	dBm	
Receiver						
Wavelength(Each Lane)	λ	840	850	860	nm	
Data rate per Lane	DR		10.3125		Gbps	
Average Power at Receiver, each Lane	-	-9.5	-	2.4	dBm	
Rx OMA per Lane	OMA	-	-	3	dBm	
Stressed Receiver Sensitivity OMA (Each Lane)	SRS	-	-	-5.4	dBm	
Peak Power(Each lane)	-	-	-	4	dBm	
Receiver Reflectance	RX_R	-	-	-12	dB	
LOS Assert	LOS_A	-30	-	-	dBm	
LOS De-Assert	LOS_D	-	-	-12	dBm	
LOS Hysteresis	-	0.5	-		dB	

Note: Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps, BER≤10^{-12}.

High Speed Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	3.135		3.465	V	
Supply Current	Icc			450	mA	
Input Differential Impedance		90	100	110	Ω	
Differential Data Input Swing	$V_{IN, P-P}$	300	-	1100	mVpp	
Differential Data Output Swing	$V_{out, P-P}$	300		850	mVpp	
Input Logic Level High		2		Vcc		
Input Logic Level Low		0		0.8		
Output Logic Level High		Vcc-0.5		Vcc		
Output Logic Level Low		0		0.4		

2-Wire Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Host 2-Wire Vcc Voltage	Vcc_Host_2w	3.14	-	3.46	V	
SCL and SDA Voltage	V_OL	0	-	0.4	V	
	V_OH	Vcc_Host_2w-0.5	-	Vcc_Host_2w+0.3	V	
	V_IL	-0.3	-	VccT*0.3	V	
	V_IH	VccT*0.7	-	VccT+0.5	V	
Input Current on the SCL and SDA Contacts	Ii	-10	-	10	mA	

2-Wire Timing Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Clock Frequency	f_scl	100		400	kHZ	1
Clock Pulse Width Low	t_low	1.3		-	μs	
Clock Pulse Width High	t_high	0.6		-	μs	
Time Bus Free before New Transmission Can Start	t_buf	20		-	μs	2
START Hold Time	t_HD,STA	0.6		0	μs	
START Set-up Time	t_SU,STA	0.6		-	μs	
Data In Hold Time	t_HD,DAT	0		-	μs	
Data In Set-up Time	t_SU,DAT	0.1		-	μs	
Input Rise Time(100kHz)	tr,100	-		1000	ns	3
Input Rise Time(400kHz)	tr,100	-		300	ns	3
Input Fall Time(100kHz)	tf,100	-		300	ns	4
Input Fall Time(400kHz)	tf,400	-		300	ns	4
STOP Set-up Time	t_SU,STO	0.6		-	us	

Notes:

1. Module shall operate with fSCL up to 100 kHz without requiring clock stretching. The module may clock stretch with fSCL greater than 100 kHz and up to 400 kHz.
2. Between STOP and START and between ACK and ReSTART.
3. From (VIL,MAX-0.15) to (VIH,MIN+0.15).
4. From (VIH,MIN+0.15) to (VIL,MAX-0.15).

Memory Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold			500	µs	1
Complete Single or Sequential Write up to 4 Byte	tWR			40	ms	
Complete Sequential Write of 5 to 8 Byte	tWR			80	ms	
Endurance (Write Cycles)		10K	-	-	ms	

Note: Maximum time the QSFP+ module may hold the SCL line low before continuing with a read or write operation.

Ordering Information

Product Name	Product Description
QSFP-AQMP-85-01	QSFP+ Plug-in, 40Gbps SR4, 100m on OM3 MMF or 150m on OM4 MMF, MPO, TX/RX 850nm, with DOM
JQ-AQMP-85-01	QSFP+ Plug-in, 40Gbps SR4, 100m on OM3 MMF or 150m on OM4 MMF, MPO, TX/RX 850nm, with DOM, Compatible with Juniper

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Ver. ACT_QSFP-AQMP-85-01_Datasheet_V2a_Dec_2023