800G QSFP-DD to QSFP-DD Active Electrical Cable

QSFP-DD Series

- QSFP-DD to QSFP-DD 800G Application
- Hot Pluggable
- Host and line interface
- Performance monitor in features
- Comprehensive test and debug capabilities
- RoHS Compliance

Ascent's 800G QSFP-DD to QSFP-DD Active Electrical Cable (AEC) is a high-performance, low-latency copper interconnect solution designed for next-generation AI infrastructure, cloud data centers, high-performance computing (HPC), and hyperscale Ethernet networks. The cable integrates advanced DSP retimer technology to extend copper transmission distance while maintaining excellent signal integrity, enabling reliable 800Gb/s connectivity between servers, switches, storage systems, and GPU clusters.

The AEC features QSFP-DD connectors on both ends and supports an aggregate data rate of 800Gb/s (8 × 106.25Gb/s PAM4) over a single cable assembly. Integrated signal conditioning and retiming technology compensate for channel loss, improve eye margin, and ensure robust transmission performance over longer copper links compared with passive DAC solutions. Operating from a 3.3V power supply, the cable supports hot-pluggable operation and provides comprehensive diagnostics, including PRBS generation and checking, loopback testing, signal-to-noise ratio (SNR) monitoring, eye histogram analysis, and advanced performance monitoring for simplified deployment and maintenance.

Designed in accordance with the QSFP-DD MSA and CMIS 5.0 specifications, the Ascent 800G AEC delivers a compact, energy-efficient, and cost-effective interconnect solution for high-density networking environments. The cable supports 800G Ethernet applications and is backward compatible with 400G and 200G operating modes, making it an ideal choice for AI clusters, Ethernet switches, storage networks, and next-generation data center architectures requiring reliable medium-reach electrical interconnects.

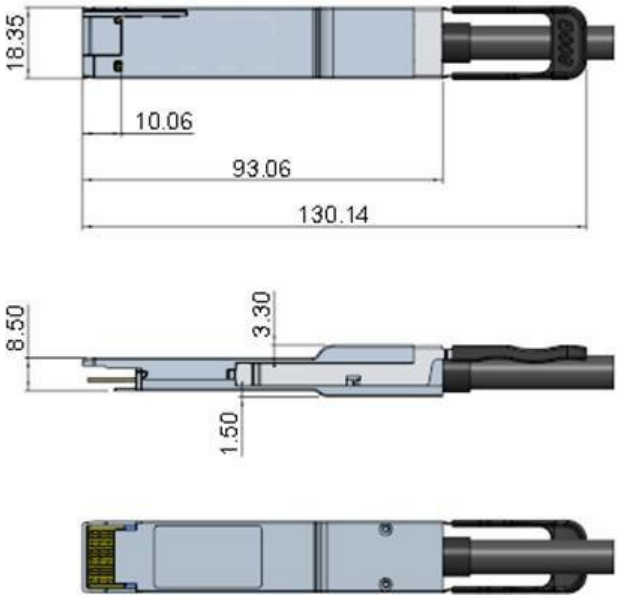
Key Features

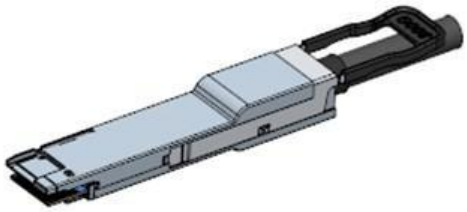
- QSFP-DD to QSFP-DD 800G Application
- 3.3V Power Supply
- Hot Pluggable
- Host and line interface support loopbacks and PRBS generator/checker for diagnostic operations
- Performance monitor in features including SNR, eye histogram and more
- Comprehensive test and debug capabilities
- RoHS Compliance
- BER<10-8(Pre FEC)*
- BER<10-15(Post FEC)*

  * Tested with QPRBS31 pattern

Outline Dimension

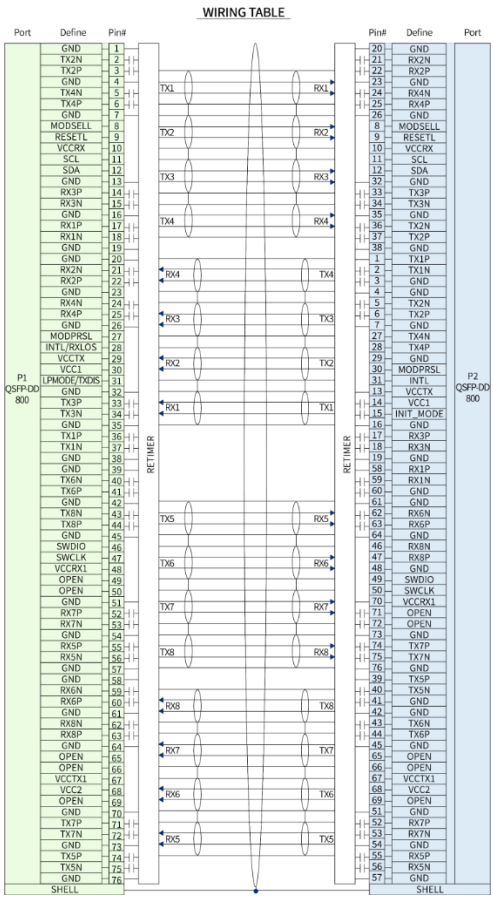
Unit:mm



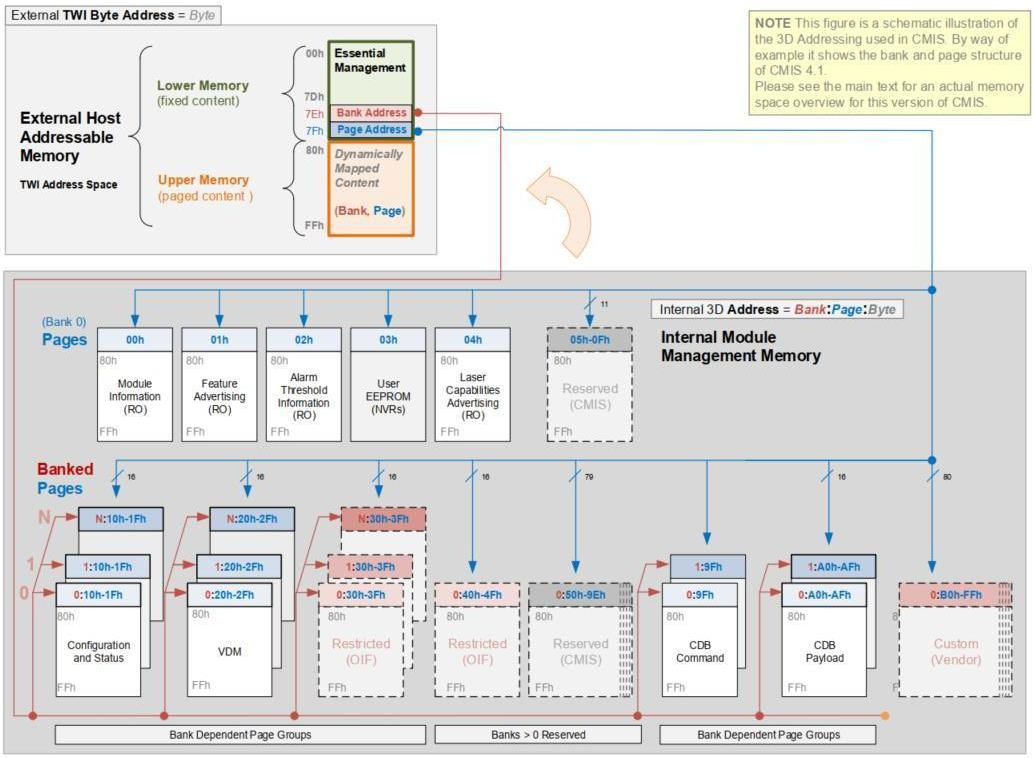


Unit:mm

Cable Wiring



Memory Map and Control Register (Compatible CMIS 5.0)



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	T_{stg}	-40	-	+85	°C	
Supply Voltage	V_{cc}	-0.3	-	3.6	V	
Relative Humidity	RH	10%	-	85%	%	Non-Condensing

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	T_{CASE}	0	-	+70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.465	V	
Power Consumption	P_{DISS}	-	-		W	
Operating Relative Humidity		0		85	%	

General Product Characteristics

Parameter	Description	
	P1 End	**P2 End**
Module Form Factor	QSFP-DD800	QSFP-DD800
Full/Half Active Full	Full Active	
Default Data Rate	800G(8*112G-PAM4) to 800G(8*112G-PAM4)	
Number of Data Lanes /Data Rate	8Lane(16Pair)/112G PAM4	
Cable Construction	Expando over discrete twinax and metal braid	
Module DSP Mode (Host to Line Side)	Retimer 8*10G to 8*100G	Retimer 8*100G to 8*100G
DSP Model	Marvell Lynx800	Marvell Lynx800
Management Interface	CMIS 5.0	CMIS 5.0
Nominal Data Rate per Lane	106.25Gbps(PAM4), KP4 FEC must be enabled	106.25Gbps(PAM4), KP4 FEC must be enabled
Pre-FEC Bit Ratio (Test with PRBS31 Patent)	<1e-8	<1e-8
Post-FEC Bit Ratio	<1e-15	<1e-15
Power Consumption per End	11W	11W
Host Max I2C Interface	400kbps	
Time to CMIS Ready	100milliseconds	
Time to Link	15seconds	
Hot Swappable/Pluggable	Yes	
Data Rate Capabilities	800G: 112G PAM4 (data rate=106.25Gbps) 400G: 56G PAM4 (data rate=53.125Gbps) 200G: 25G NRZ (data rate=25.78125Gbps)	

Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Note
Characteristic Impedance	90	100	110	ohm	
Time Propagation Delay (Informative)			4.9	ns	

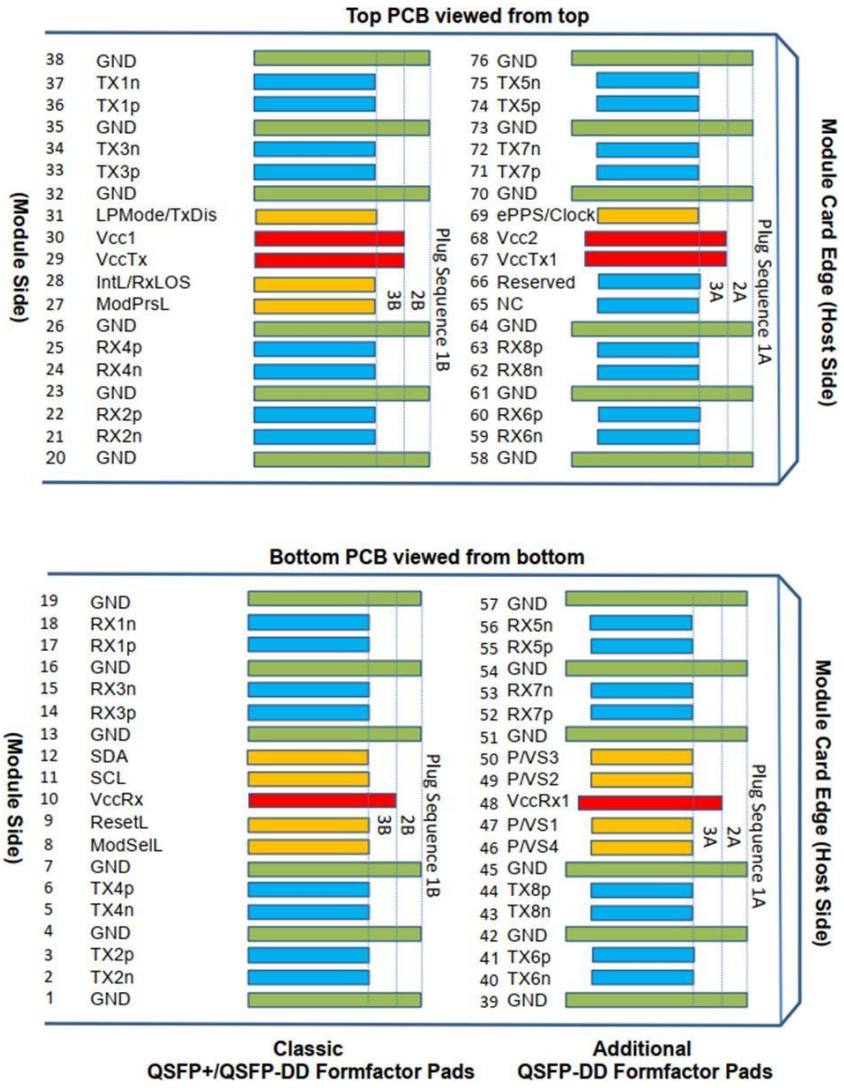
Low Speed Electrical Signal

Parameter	Symbol	Min.	Max.	Unit	Note
Module Output SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	V_{CC}-0.5	V_{CC}+0.3	V	
Module Input SCL and SDA	VOL	-0.3	Vcc*0.3	V	
	VOH	V_{CC}*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total Bus Capacitive Load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor, max
			200	pF	1.6k Ohms Pull up resistor, max
LPMode/TxDis,Reset and ModeSeIL	VIL	-0.3	0.8	V	|Iin|</=125uA for Vin < Vcc
	VIH	2	V_{CC}+0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	V_{CC}-0.5	V_{CC}+0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can implemented as a short-circuit to GND on the module

Digital Diagnostics

Parameter	Symbol	Unit	Accuracy	Notes
Temperature Monitor Absolute	DMI_TEM	˚C	±3	Over Operating Temp
Supply Voltage Monitor Absolute	DMI _VCC	V	±5	Full Operating Range

Pin Assignment



Pin	Logic	Symbol	Description	PlugSeq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I		ModselL	3B	
9	LVTLL-I		ResetL	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1

Pin	Logic	Symbol	Description	PlugSeq.	Notes
14	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx1n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/Optional Rx LOS	3B	
29		VccTx	+3.3 V Power Supply Transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power Mode/Optional Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	

Pin	Logic	Symbol	Description	PlugSeq.	Notes
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP- DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector(see MSA specification). For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000mA.

Note 3: Reserved pad recommended to be terminated with 10kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10kΩ to ground on the host.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP- DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10kΩ.

Note 6: For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

Handling Precautions

This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety

Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

Ordering Information

Product Name	Product Description
Q112-DD-AEC-002	QSFP-DD to QSFP-DD 800G AEC w/Marvell Lynx800 DSP, 32AWG, 2.0M
Q112-DD-AEC-003	QSFP-DD to QSFP-DD 800G AEC w/Marvell Lynx800 DSP, 30AWG, 3.0M
Q112-DD-AEC-004	QSFP-DD to QSFP-DD 800G AEC w/Marvell Lynx800 DSP, 28AWG, 4.0M
Q112-DD-AEC-005	QSFP-DD to QSFP-DD 800G AEC w/Lynx800 DSP, 28AWG, 5.0M

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Ver. ACT_Q112-DD-AEC-XXX_Datasheet_V1b_Jul_2025