

400G QSFP-DD DCO ZR Optical Transceiver

QSFP-DD Series



- **QSFP-DD MSA compliant**
- **Client signal 400GbE or 4x100GbE**
- **Line Modulation format 400G DP-16QAM**
- **Ingress LF hold-off time configure**
- **Hitless firmware upgrade**
- **Maximum power consumption 18W**
- **Duplex LC Receptacle**
- **RoHS compliant**

The ACT QDD-400G-ZR Series is a high-performance coherent optical transceiver designed for 400GbE data center interconnect (DCI), metro transport, and high-capacity backbone networks. Utilizing advanced coherent DSP technology and tunable C-band DWDM optics, the module enables transmission distances of up to 120 km without inline chromatic dispersion compensation, providing a compact and cost-effective solution for next-generation optical transport networks.

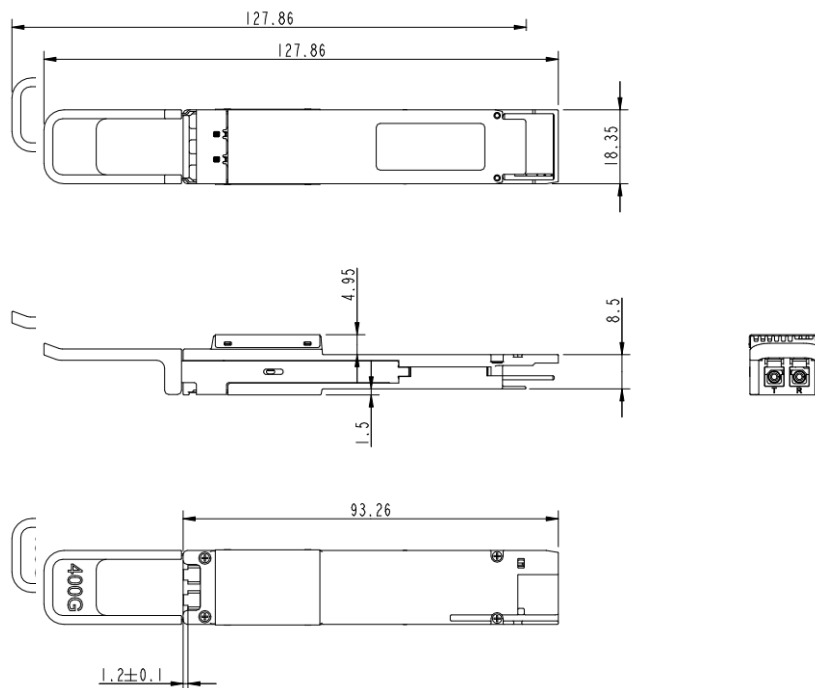
The transceiver integrates a state-of-the-art 7 nm coherent DSP, ultra-narrow linewidth tunable lasers, high-speed modulators, and coherent receivers to deliver exceptional optical performance with 400G DP-16QAM modulation. Supporting both 400GbE and 4x100GbE client interfaces, the module offers flexible deployment across data center, carrier, and enterprise networks while reducing operational complexity and power consumption.

Compliant with the QSFP-DD MSA and OIF 400ZR specifications, the QDD-400G-ZR supports comprehensive digital diagnostics, hot-pluggable operation, and seamless integration into modern switching and routing platforms. Its compact form factor, low power consumption, and Juniper-compatible option make it an ideal solution for DCI, metro, and cloud network applications.

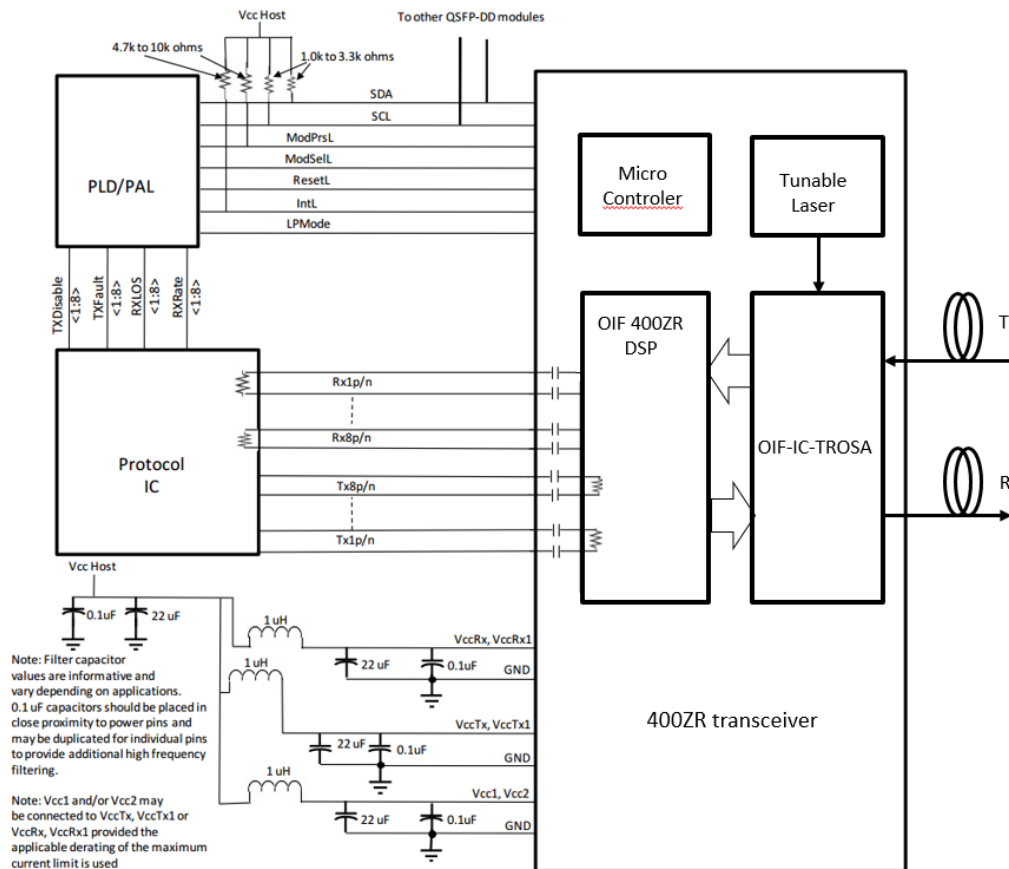
Key Features

- QSFP-DD MSA compliant type 2B package
- Up to 120km transmission distance
- Client signal 400GbE or 4x100GbE
- Line Modulation format 400G DP-16QAM
- C-band tunable, supports 100/75GHz grid spacing, support 0.1GHz fine turning
- TX power -13dBm to -9dBm tunable
- Support ingress LF hold-off time configure
- Support hitless firmware upgrade
- Compact size (18.35 mm x 93.26 mm x 8.50 mm)
- Duplex LC Receptacle
- Operating case temperature: 0°C to 75°C
- Maximum power consumption 18W (400GbE)
- Single 3.3 V power supply
- RoHS 2 compliant

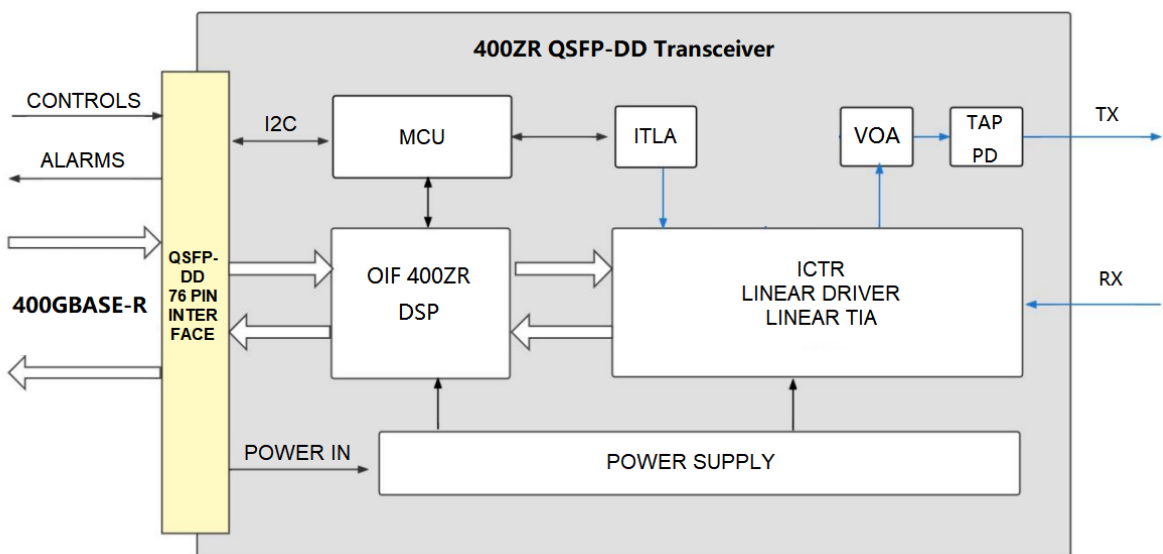
Mechanical Dimensions



Recommended Interface Circuit



Block Diagram of Transceiver



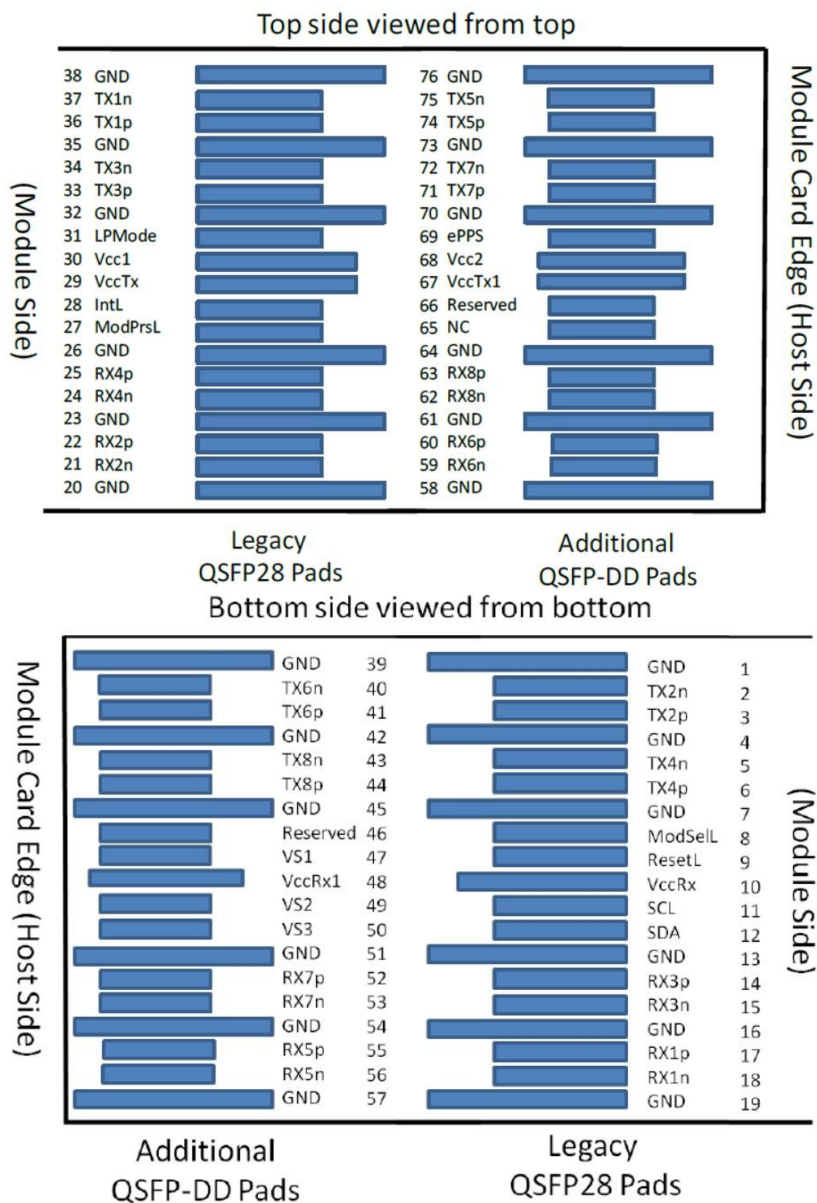
EEPROM Information

Parameter	Unit	Threshold	Description
Temp Low Warning	°C	0	Min. case temperature
Temp High Warning	°C	75	Max. case temperature
Voltage Low Warning	V	3.135	-5% Vcc target
Voltage High Warning	V	3.465	+5% Vcc target
Tx Power Low Warning	dBm	-15	OIF 400ZR app code 0x01/03
		-9	OIF 400ZR app code 0x02
Tx Power High Warning	dBm	-6	
Rx Power Low Warning	dBm	-22	
Rx Power High Warning	dBm	2	
Laser Temp Low Warning	°C	0	
Laser Temp High Warning	°C	70	
Temp Low Alarm	°C	-10	
Temp High Alarm	°C	85	
Voltage Low Alarm	V	2.97	
Voltage High Alarm	V	3.63	
Tx Power Low Alarm	dBm	-18	OIF 400ZR app code 0x01/03
		-12	OIF 400ZR app code 0x02
Tx Power High Alarm	dBm	-4	
Rx Power Low Alarm	dBm	-24	
Rx Power High Alarm	dBm	6	
Optional Laser Temp Low Alarm	°C	-10	
Optional Laser Temp High Alarm	°C	80	

Digital Diagnostic Functions

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Over operating temp
TX Power Monitor absolute Error	DMI_TX	-1/-1.5	1/1.5	dB	-15 to -9 dBm
					±1dB@(25 to 60) °C ±1.5dB@(0 to 75) °C
RX Power Monitor Absolute Error	DMI_RX	-1.5/-2	1.5/2	dB	±1.5dB @ (-12 to 0) dBm
					±2dB @ (-20 to 0) dBm
Supply Voltage Monitor Absolute Error	DMI_VCC	-3	3	%	
Bias Current Monitor Absolute Error	DMI_Ibias	-10	10	%	
No-Power Monitor RX		-40		dBm	
Tx_Disable Power Monitor		-40		dBm	

Pin Assignment



Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	

Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMODE	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1

Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input. Not used	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	

Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Block Diagram of Transceiver for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40		85	°C	
Power Supply	Vcc	-0.3	3.3	3.6	V	Not damaged
Relative Humidity	RH	5		85	%	Non-condensing
Receiver Damage Threshold	PRdmg	10			dBm	Total optical power
ESD Sensitivity				1000	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	Tc	0		75	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
	Icc			6.1	A	1
Maximum Sustained Peak Current(<500ms)				6.3	A	
Maximum Instantaneous Peak Current(<50us)				7.6	A	
Electro-Static Discharge	ESD			1000	V	
Power Consumption	PD			18	W	1
Relative Humidity	RH	15		85	%	
Client Mode		1 x 400GAUI-8 (OIF-400ZR-02.0) 4 x 100GAUI-2				
Transmission Distance			80	120	Km	30 to 40Km unamplified P2P link
Power Supply Noise	Vrip			1%	DC-1MHz	
				2%	1-10MHz	

Note. Maximum power consumption is 18W in 400GbE mode. In 4x100GbE mode, the maximum power consumption will be 19W, and the current will also change accordingly.

Optical Electrical Characteristic

Tested under recommended operating conditions, unless otherwise noted

Parameters	Min.	Typ.	Max.	Unit	Note
Modulation Format	ZR400-CFEC-16QAM				CFEC FEC, NCG 10.8dB SFF-8024 Media ID 3Eh/3Fh
Baud Rate	59.843750000±20ppm				
Transmitter Frequency Range	191.3		196.1	THz	OIF 400ZR app code 0x01/03
		193.7		THz	OIF 400ZR app code 0x02, fixed wavelength
Flexible DWDM Grid	3.125			GHz	OIF 400ZR app code 0x01/03
Frequency Fine Tuning Range	-5		5	GHz	bright tuning, OIF 400ZRapp code 0x01/03
Frequency Fine Tuning Step	0.1			GHz	OIF 400ZR app code 0x01/03

Parameters	Min.	Typ.	Max.	Unit	Note
Laser Frequency Accuracy	-1.8		1.8	GHz	
TX Spectral Upper Mask			(30.0, 0.0) (37.0,-10.0) (39.2,-15.0) (40.4,-20.0)	(GHz,dB)	Refer to OIF-400ZR-02.0 13.3.201a
TX Spectral Lower Mask	(30.0,-9.0) (31.3,-20.0) (31.3,-35.0)			(GHz,dB)	Refer to OIF-400ZR-02.0 13.3.201b
Transmitter Laser Disable Time			100	ms	
Transmitter Wavelength Wwitching Time			60	s	
Transmitter Laser Enable Time			10	s	
Tx Output Power(at Program Output Power Max)	-10		-6	dBm	At Programmed Output Power Max, transmit output power over wavelength, temperature, and aging. 0x01/03–400ZR,DWDM amplified
	-9		-6	dBm	193.7THz, 0x02–400ZR,Single wavelength, unamplified
Transmit Output Power Adjustable Range	-13		-9	dBm	The absolute accuracy is ±1dB OIF 400ZR app code 0x01/03
Transmit Output Power Adjust Step	0.1			dB	OIF 400ZR app code 0x01/03
Optical Power Setting Accuracy	-1		1	dB	Diff between setting and reporting
Output Power Monitor Accuracy	-1		1	dB	
Power Stability			0.5	-0.5	At fixed wavelength, room temp
			1	-1	At fixed wavelength, environment temp
Total Output Power with Tx Disabled			-20		
Total Output Power During Wavelength Switching			-20		
Transmitter Reflectance			-20		Looking into the Tx

Parameters	Min.	Typ.	Max.	Unit	Note
Inband (IB) OSNR				40	
Out-of-Band (OOB) OSNR				35	
Lorentzian Linewidth			300		Tx and LO
Relative Intensity Noise			-140		
Mean I-Q Amplitude Imbalance			1		
Transmitter Polarization Dependent Power			1.5		
DC I-Q Offset (Mean per Polarization)			-26		
I-Q Instantaneous Offset			-20		
Receiver Operating Characteristic-Optical					
Parameter	Min.	Typ.	Max.	Unit	Note
Modulation Format	ZR400-CFEC-16QAM				CFEC FEC, Net Coding Gain(NCG) 10.8dB
Baud Rate	59.843750000±20ppm				
Frequency Offset between Received Carrier and LO	-3.6		+3.6	GHz	
Input Power Range	-12		0	dBm	Signal power of the channel for the 26dB OSNR tolerance 0x01–400ZR,DWDM amplified 193.7THz,0x02–400ZR,Single wavelength, unamplified
	-20		0	dBm	
OSNR Tolerance			26	dB/0.1nm	
RX Sensitivity	-20			dBm	
Non-Damaging Input Power			10	dBm	
Optical Input Power Monitor Accuracy	-2		2	dB	Inband (IB) OSNR ≥ 34dB Total power
MAX Pre-FEC BER	0.01		0.0125		
Chromatic Dispersion Tolerance			2400	ps/nm	
CD Monitor Accuracy	-200		200	ps/nm	
Average PMD (DGD) Tolerance	10(33)			ps	
DGD Monitor Accuracy	-15		15	ps	OSNR penalty < 0.5dB, when change in SOP is < 1 rad/ms. OSNR penalty<0.5dB 0~40ps Tolerance to peak PDL with < 1.8 dB penalty to OSNR tolerance (13.3.330) when change in SOP is < =1 rad/ms. Test configuration: PDL emulator applied before noise loading. With <0.5 dB OSNR penalty Optical reflectance at Rx connector input. OIF 400ZR app code
Peak PDL Tolerance			3.5	dB	
Tolerance to Change in SOP	50			krad/s	
Optical Return Loss	20			dB	
Optical Rx_LOS Assert Threshold	-28	-26	-24	dBm	

Parameter	Min.	Typ.	Max.	Unit	Note
Optical Rx_LOS Hysteresis	1	1.5	2.5	dB	0x01, 0x02, 0x03
Optical Input Power Transient Tolerance	-2		2	dB	Tolerance to change in input power with < 0.5 dB penalty to OSNR tolerance. The 20% to 80% rise/fall times for the input power change shall be no faster than 50 μ s.
Service Recovery Time			40	ms	

Note: The transmitter and receiver comply with the 400GAUI-8 C2M and CEI-56G-VSR-PAM4 electrical specification, electrical interface definitions refer to IEEE Std 802.3-2018 Annex 120E. The data lines are AC-coupled and terminated in the module per the following figure from the QSFP-DD MSA.

Operating Characteristic-Electrical High Speed

Parameter	Symbol	Min	Max	Unit	Note
400GAUI-8 C2M Electrical Characteristics					
Transmitter(Module Output)					
Signaling Rate, each Lane		26.5625 $\pm$ 100 ppm		GBd	PAM-4
AC Common-Mode Output Voltage (RMS)	RMS		17.5	mV	
Differential Voltage Pk-Pk	Vin, pp	750	900	mV	
Near-End ESMW (Eye Symmetry Mask Width)		0.265		UI	
Near-End Eye Height, Differential		70		mV	
Far-End ESMW		0.2		UI	
Far-End Eye Height, Differential		30		mV	
Far-End Pre-Cursor ISI Ratio		-4.5	2.5	%	
Differential Output Return Loss		Equation (83E-2)			IEEE Std 802.3-2018 Annex 120E
Common to Differential Mode Conversion Return Loss		Equation (83E-3)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch		-	10	%	At 1 MHz
Transition Time(20% to 80%)	Trise/Tfall	9.5		Ps	20% to 80%
DC Common Mode Voltage	Vcm	-350	2850	mV	
Receiver (Module Input)					
Signaling Rate per Lane		26.5625 $\pm$ 100 ppm		GBd	PAM-4
Differential Pk-Pk Input Voltage Tolerance	Vout, pp	900		mV	
Differential Input Return Loss (Min)		Equation (83E-5)			IEEE Std 802.3-2018 Annex 120E

Parameter	Symbol	Min	Max	Unit	Note
Differential to Common-Mode Input Return Loss (Min)		Equation (83E-6)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	
Module Stressed Input Test		See 120E.3.4.1			IEEE Std 802.3-2018 Annex 120E
Single-Ended Voltage Tolerance Range (Min)		-0.4	3.3	V	
DC Common Mode Voltage(Min)		-350	2850	mV	

Operating Characteristic-Electrical Low Speed

Parameter	Symbol	Min	Max	Unit	Note
SCL and SDA	VOL	0.4	V	0	IOL(max)=3mA for fast mode, 20ma for Fast-mode plus
SCL and SDA	VOH	V _{CC} +0.3	V	V _{CC} -0.5	
	VIL	V _{CC} *0.3	V	-0.3	
	VIH	V _{CC} +0.5	V	V _{CC} *0.7	
Capacitance for SCL and SDA I/O Signal	Ci	14	pF		
Total Bus Capacitive Load for SCL and SDA	Cb	100	pF		For 400kHz clock rate, use 3.0 k Ohms Pull up resistor max. For 1000kHz clock rate, refer to Figure 45 (QSFP-DD-Hardware-rev5p0)
		200	pF		
InitMode, ResetL and ModSelL	VIL	0.8	V	-0.3	0V<Vin<V _{CC} IOL=2.0mA 10k ohms pull up to Host V _{CC} IOL=2.0mA ModPrsL can be implemented as a short-circuit to GND on the module
	VIH	V _{CC} +0.3	V	2	
	I _{in}	360	uA		
	VOL	0.4	V	0	
	VOH	V _{CC} +0.3	V	V _{CC} -0.5	
ModPrsL	VOL	0.4	V	0	
	VOH				

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Max	Unit	Note
MgmtInit Duration	Max MgmtInit		2000	ms	1
ResetL Assert Time	t_reset_init	10		us	2
IntL Assert Time	ton_IntL		200	ms	3
IntL Deassert Time	toff_IntL		500	us	4
Rx LOS Assert Time	ton_los		100	ms	5
Rx LOS Assert Time (Optional Fast Mode)	ton_losf		10	ms	6
Rx LOS Deassert Time	toff_los		100	ms	
Tx Fault Assert Time	ton_Txfault		200	ms	7
Flag Assert Time	ton_flag		200	ms	8
Mask Assert Time	ton_mask		100	ms	9
Mask Deassert Time	toff_mask		100	ms	10
High Power Up State			180	s	
Software TX Disable Assert Time			100	ms	
Software TX Disable De- Assert Time			10	s	

Notes

1. Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
4. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
5. Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
6. Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
7. Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
8. Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
9. Time from mask bit set (value=1b) until associated IntL assertion is inhibited.
10. Time from mask bit cleared (value=0b) until associated IntL operation resumes.

IIC 2-Wire Characteristics

Parameter	Symbol	Fast Mode (400 KHz)		Fast Mode Plus(1 MHz)		Unit	Conditions
		Min	Max	Min	Max		
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.5		μs	
Clock Pulse Width High	tHIGH	0.6		0.26		μs	
Time Bus Free before New Transmission Can Start	tBUF	20		1		μs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		μs	The delay required between SDA becoming low and SCL starting to go low in a START

Parameter	Symbol	Fast Mode (400 KHz)		Fast Mode Plus(1 MHz)		Unit	Conditions
		Min	Max	Min	Max		
START Setup Time	tSU.STA	0.6		0.26		μs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		μs	
Data In Setup Time	tSU.DAT	0.1		0.1		μs	
Input Rise Time	tR		300		120	ns	
Input Fall Time	tF		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH,MIN=0.7*Vcc)
STOP Setup Time	tSU.STO	0.6		0.6		us	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Hold Time	tHD.STO	0.6		0.26		us	
Aborted Sequence-Bus Release	Deselect _Abort	2		2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time1	tSU.Mod Sell	2		2		ms	ModSelL Setup Time is the setup time on the select lines before the start of a host initiated serial bus sequence
ModSelL Hold Time1	tHD.Mod Sell	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single Sequential Write	tWR		40		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50K		50K		cycles	Module Case Temperature = 75°C

Note: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.

Ordering Information

Product Name

QDD-400G-ZR

JQDD-400G-ZR+HP

Product Description

QSFP DD 400G PM-16QAM Plug-in, Coherent ZR Optical Transceiver, up to 120km with amplification, Duplex, LC, DOM

QSFP DD 400G OpenZR+ High Power Coherent JCO400-QDD-ZR-M-HP ZR+, Optical Transceiver, LC, DOM, Juniper Compatible

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Specifications and product availability are subject to change without notice.
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