200 Gb/s QSFP DD LR4 10 km Transceiver

QSFP-DD Series

- 200GBASE-LR4
- Lane bit rate 53.125 Gb/s with PAM4
- Up to 10km transmission on SMF
- Compliant with IEEE 802.3cn 200GBASE-LR4
- Single +3.3V power supply
- Maximum power consumption 10W
- Complies with EU Directive 2015/863/EU

The ACT QDD-200-LR4-LP10 is a high-performance 200 Gb/s QSFP-DD optical transceiver designed for next-generation data center and service provider networks requiring high bandwidth and extended reach. Supporting 200GBASE-LR4 with four LAN-WDM wavelengths over single-mode fiber, the module enables reliable transmission distances of up to 10 km, making it well suited for data center interconnect (DCI), metro aggregation, and high-capacity enterprise applications.

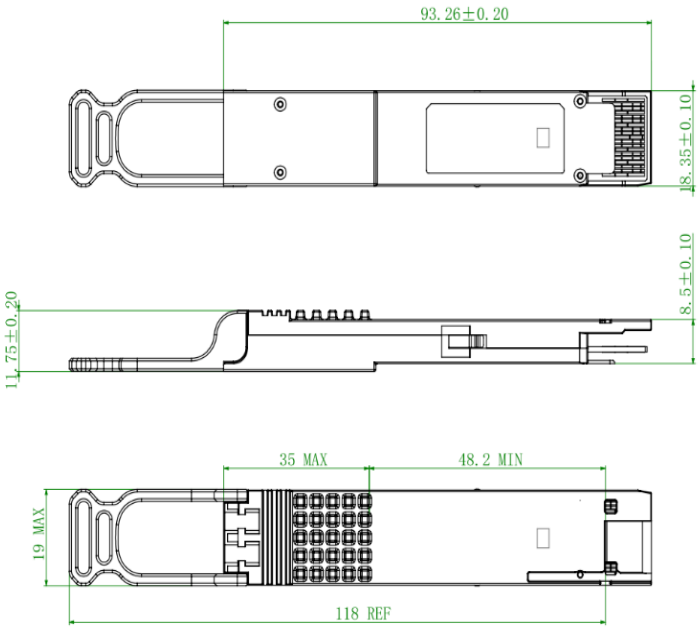
Built on PAM4 modulation with a lane data rate of 53.125 Gb/s, the transceiver complies fully with IEEE 802.3cn 200GBASE-LR4, QSFP-DD MSA, and CMIS standards, ensuring broad interoperability with leading network platforms. The module integrates LAN-WDM lasers and PIN receivers in a compact QSFP-DD form factor with LC duplex connector, while maintaining a maximum power consumption of 10 W for efficient thermal performance in high-density environments.

Designed for operational reliability, the ACT QDD-200-LR4-LP10 supports comprehensive Digital Diagnostic Monitoring (DDM), allowing real-time access to critical parameters such as temperature, voltage, bias current, and optical power. With the compliance with EU Directive 2015/863/EU (RoHS), this transceiver provides a robust, standards-based solution for scalable 200G optical deployments.

Key Features

- Supports 200GBASE-LR4
- Lane bit rate 53.125 Gb/s with PAM4
- Up to 10km transmission on SMF
- LAN WDM laser and PIN receiver
- 200GAUI-8 Electrical interface with 8 Lanes 26.5625Gb/s NRZ high-speed signal
- QSFP-DD MSA package with duplex LC connector
- Compliant with IEEE 802.3cn 200GBASE-LR4
- Single +3.3V power supply
- Maximum power consumption 10W
- Operating case temperature: 0 to +70 °C
- Compliant to QSFP-DD CMIS & QSFP-DD MSA HW standard
- Complies with EU Directive 2015/863/EU

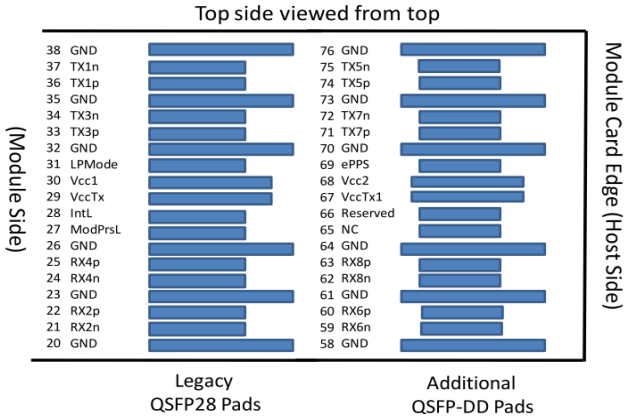
Outline Diagram

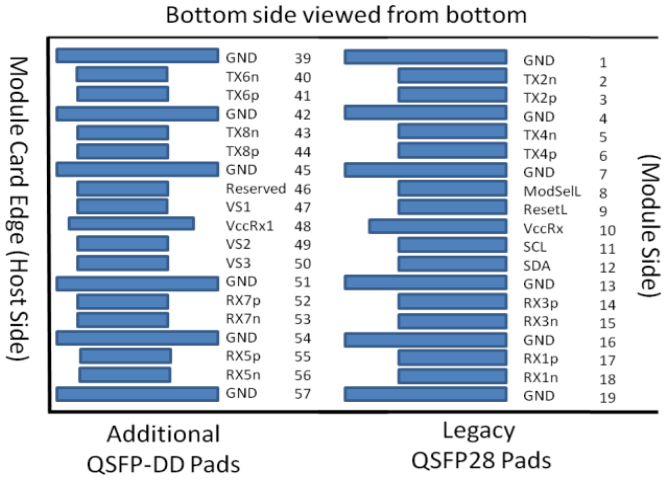


Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V_{CC}	±3%	V	Internal
Tx Bias Current Per Lane	0 to 100	±10%	mA	Internal
Tx Output Power Per Lane	-3.4 to 5.3	±3	dBm	Internal
Rx Power per lane	-9.7 to 5.3	±3	dBm	Internal

Pin Assignment





Pin	Logic	Symbol	Description	Plug Seq.	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2

Pin	Logic	Symbol	Description	Plug Seq.	Note
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/Rx LOS	3B	
29		VccTx	+3.3 V Power Supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	

Pin	Logic	Symbol	Description	Plug Seq.	Note
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see above figure for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	T_S	-40	-	85	°C	
Supply Voltage	V_{CC}	-0.5	-	3.6	V	
Operating Relative Humidity	RH	-	-	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	T_C	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Power Supply Current	I_{CC}	-	-	3.03	A	3.3V
Power Consumption	P	-	-	10	W	
Aggregate Bit Rate	BR_{AVE}	-	212.5	-	Gb/s	With PAM4
Lane Bit Rate	BR_{LANE}	-	53.125	-	Gb/s	With PAM4
Transmission Distance	TD	-	-	10	km	Over SMF

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Signaling Rate, each Lane	BR	26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Lane Wavelengths	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side-Mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	P_{MAX}	-	-	11.3	dBm	
Average Launch Power, each Lane	P_{OUT}	-3.4	-	5.3	dBm	1
Outer OMA, each Lane	OMA_{outer}	-0.4	-	5.1	dBm	2
Difference in Launch Power between Lanes (OMA)		-	-	4	dB	
Transmitter and Dispersion Eye Closure for PAM4	TDECQ	-	-	3.2	dB	
Average POUT (Laser Turn Off)	P_{OFF}	-	-	-30	dBm	
Extinction Ratio, each Lane	ER	3.5	-	-	dB	
Receiver						
Signaling Rate, each Lane	BR	26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Lane Wavelengths	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	P_{DAMAGE}	6.3	-	-	dBm	3
Average Receive Power, each Lane	P_{RX_LANE}	-9.7	-	5.3	dBm	4

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Receive Power (OMAouter), each Lane	RX_{OMA}	-	-	5.1	dBm	
Receiver Sensitivity (OMAouter), each Lane	SEN_{OMA}	-	-	-7.2	dBm	5

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) must exceed this value.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at TP3 for the BER 2.4E-4.

Electrical Characteristics

High-Speed Signal: Compliant to 200GAUI-8 (IEEE 802.3bs)

Low-Speed Signal: Compliant to QSFP-DD-Hardware.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
(Module Input)						
Differential Data Input Amplitude	$V_{IN,P-P}$	900	-	-	mVpp	
Differential Termination Mismatch		-	-	10	%	
Receiver (Module Output)						
Differential Data Output Amplitude	$V_{OUT,P-P}$	-	-	900	mVpp	
Differential Termination Mismatch(1MHZ)		-	-	10	%	
Low-speed Electrical Interface						
LPMode, ResetL,	V_{IL}	-0.3	-	0.8	V	
ModSelL and ePPS	V_{IH}	2.0	-	V_{CC}+0.3	V	
ModPrsL	V_{OL}	0	-	0.4	V	
	V_{IH}	ModPrsL can be implemented as a short-circuit to GND on the module				
IntL	V_{OL}	0	-	0.4	V	
	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	

Ordering Information

Product Name	Product Description
QDD-200-LR4-LP10	QSFP DD PAM4 Plug-in, 200GBASE-LR4 10km, SMF,LC Duplex, DOM

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