400G QSFP-DD DCO ZR Coherent Optical Transceiver

QSFP-DD Series

- **Support Flex-grid channel spacing DWDM in C-band**
- **Support client-side and line-side Interfaces**
- **Support Line-side DP-16QAM with CFEC**
- **Standard QSFP-DD type 2 form factor**
- **76-pin QSFP-DD MSA compliant connector**
- **Compliant to CMIS 5.0**
- **RoHS compliant**

Ascent's QDD-400G-ZR QSFP-DD Digital Coherent Optic Modules are 400 Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) transceivers designed for long distance optical communication applications over a standard pair of G.652 Single-Mode Fiber (SMF).

The QSFP-DD DCO modules based on 400G DP-16QAM supporting extended C-band, polarization diversity coherent detection, and advanced electronic link equalization. Chromatic dispersion compensation can be applied to the receiving side of the demodulator. This module is managed to utilize the Two Wire Interface that is specified in the Common Management Interface Specification (CMIS).

The module uses a 76-pin QSFP-DD MSA QSFP-DD Hardware Specification connector for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the QSFP-DD. The module can be portioned into three functional parts: TX path, RX path and Control & Power block.

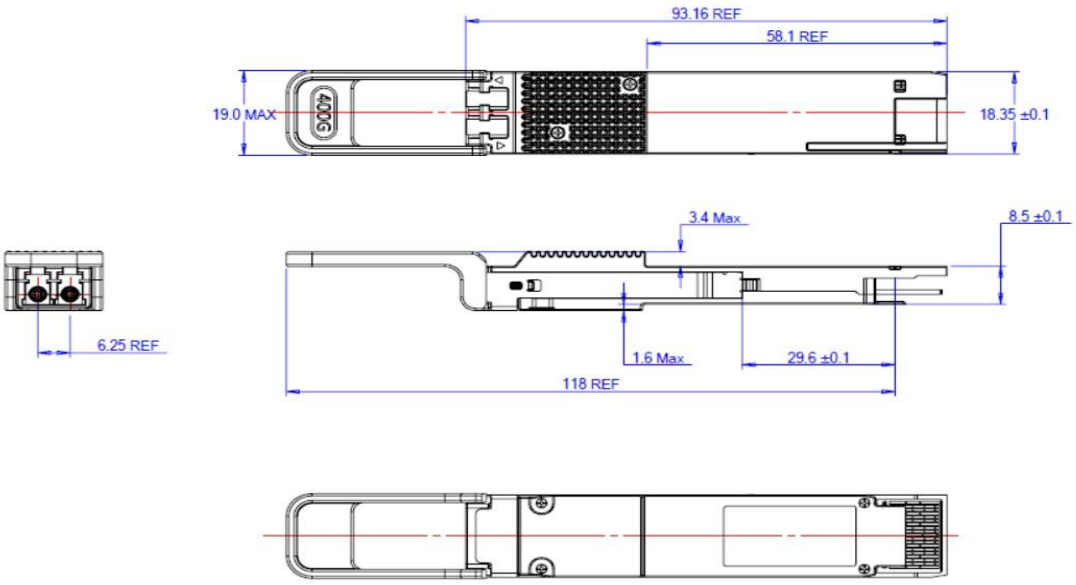
The host interface is comprised of a total of 8 high-speed SerDes lanes. This allows module to support multiple client application mode for 400GbE application.

Key Features

- Support Flex-grid channel spacing DWDM in C-band
- Support Client-side Interfaces: 400GAUI-8
- Support Line-side DP-16QAM with CFEC
- Standard QSFP-DD type 2 form factor
- 76pin QSFP-DD MSA compliant connector
- Compliant to CMIS 5.0
- Compliant to OIF Implementation Agreement for Coherent CMIS, Rev 01.1
- OIF-400ZR-01.0_reduced2.pdf
- RoHS compliant

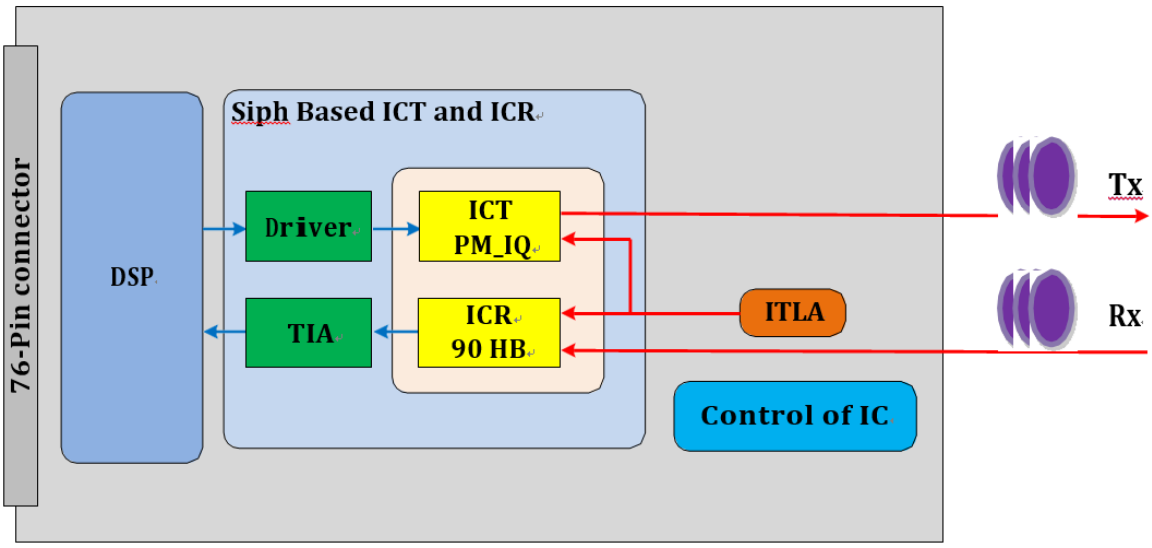
Outline Diagram

The pluggable module fully compliant with the QSFP-DD Type 2 Module Specification, including dimensions and tolerances for the connector, cage and module system. The module shall be designed to be inserted into a host board with a railing system that includes a heat sink.



Functional Diagram

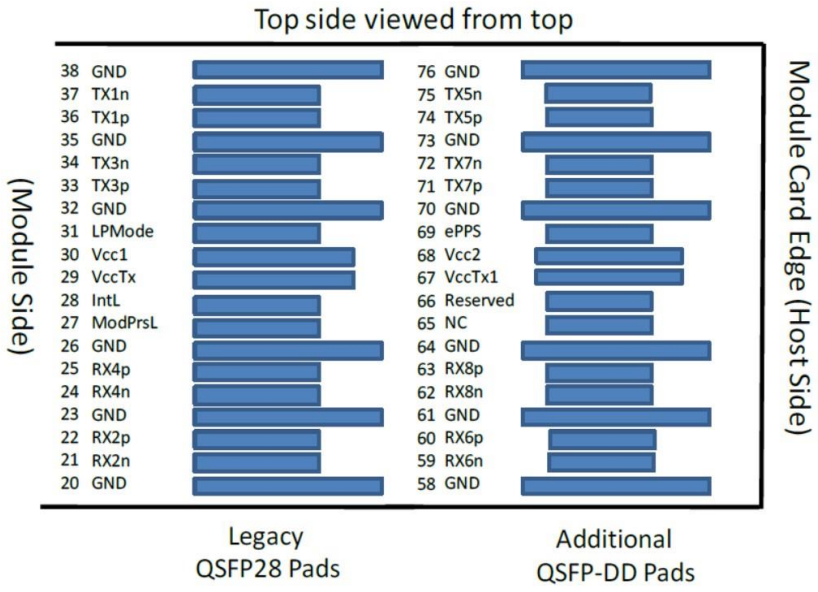
The application field of the module is widely used for short haul (ZR) to Metro (MR) interconnects. As shown in the figure below, it is comprised of high-data lanes, a single 3.3V power supply, an IIC interface for module control and status report, and dedicated alarm and control pins (not shown on the figure).

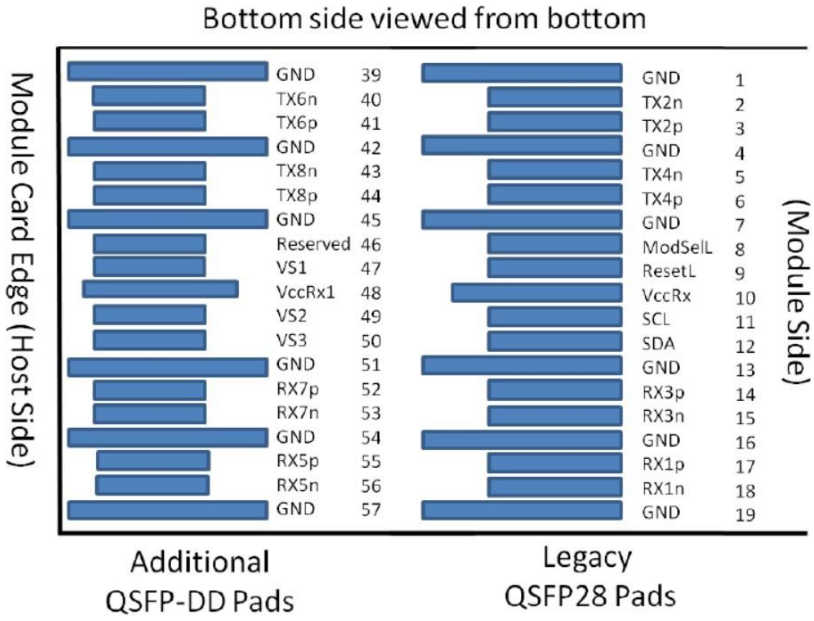


Pin Assignment

The electrical interfaces, including pad assignments for data, control, status and power supplies and host PCB layout requirements, of the module is fully compliant with the QSFP-DD MSA QSFP-DD-Hardware Specification, Rev 5.0.

The case of the QSFP-DD module is isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.





Pin #	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16		GND	Ground	1B
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B

Pin #	Logic	Symbol	Description	Plug Sequence
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

Hardware Control and Status Pins

In addition to the 2-wire serial interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- LPMode
- ModPrsL
- IntL
- ePPS

ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de - asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP -DD module. LPMode is used in the control of the module power mode.

See CMIS Section 6.3.1.3.

ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

The QSFP-DD low speed electrical specifications are given in the table below. This specification ensures compatibility between host bus masters and the 2-wire interface.

Parameter	Symbol	Min.	Max.	Unit	Note
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA for fast mode, 20 mA for Fast-mode plus
	VIL	-0.3	Vcc * 0.3	V	
	VIH	Vcc * 0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for	Cb		100	pF	For 400 kHz clock rate use 3.0 kΩ pull-up resistor, max.
SCL and SDA			200	pF	For 400 kHz clock rate use 1.6 kΩ pull-up resistor, max.
LPMode, ResetL,	VIL	-0.3	0.8	V	
ModSelL and ePPS	VIH	2	Vcc + 0.3	V	
LPMode, ResetL and ModSelL	|Iin|		360	uA	0V<Vin<Vcc
ePPS	|Iin|		TBD	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	Vcc – 0.5	Vcc + 0.3	V	10 kΩ pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0 mA
	VOH			V	ModPrsL can be implemented as a short-circuit to GND on the module

Module Configuration

Host Interface

The module support for wide applications with Host interfaces: 400GAUI-8. The Host interface conform to existing protocol standards and operate over standard physical layer specifications. The termination, mapping and/or aggregation of this signal is into an internal ZR frame structure. The ZR frame structure is then adapted to the CFEC engine and DSP framed for transmission over the coherent media Interface. The Host interface signaling conform to existing protocol and electrical standards as defined by IEEE 802.3TM-2018.

The Host Interface compliant to very short reach high speed chip-to-module electrical interface CEI-56G-VSR-PAM4 for PAM4 coding.

Host Interface	Application Data Rate	Lane Count	Lane Signaling Rate	Modulation
1*400GAUI-8	425.00 Gb/s	8	26.5625 GBaud (± 100 ppm)	PAM4

Media Interface

The media interface utilizes DP-16QAM modulation, polarization diversity coherent detection, and advanced electronic link equalization with chromatic dispersion and differential group delay compensation.

The module terminates the host interface signal then maps and aggregates them into an internal ZR frame structure. The ZR frame structure is then adapted to the CFEC engine and DSP framed for transmission over the coherent media interface.

Application Bit Rate	Baud Rate	Modulation	FEC
478.75 Gb/s	59.84375GBd	DP-16QAM	CFEC

Management Interface

The management communication interface provides a number of elementary management operations that allow the host to read from or write to byte-sized management registers in the management memory map of the module. There are read and write operations both for single bytes and for contiguous byte sequences. Two types of read operations, either with implicit addressing (read from current address) or with explicit addressing, are supported.

The management communication interface distinguishes a master role and a slave role. The host shall be the master and the module shall be the slave.

The master initiates all operations that lead to data transfer. Data can be transferred from the master to the slave (in write operations) and from the slave to the master (in read operations).

Physical Layer

The physical layer supporting communication between host and module is the Two Wire serial Interface (TWI).The TWI consists of a clock signal (SCL) and a data signal (SDA).

SCL and SDA comprise a 2-wire serial interface between the host and module using the TWI protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

Both signals (SCL and SDA) are bidirectional open-collector pins and require an external pull-up to VCC on the host PCB. Activating the line requires pulling it down (wired AND). The total capacitance on the bus should not exceed 400pF.

This 2-wire interface supports bus speeds:

- Fast mode - I2C Fast-mode (Fm) ≤ 400 kbit/s
- Fast mode plus - I2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s

The SDA signal is bi-directional. During binary data transfer, the SDA signal shall transition when SCL is low.

SDA transitions when SCL is high are used to mark either the beginning (START) or ending (STOP) of a data transfer.

Specifications

Absolute Maximum Ratings

The absolute maximum ratings given in the table below define the damage thresholds. Hence, the component shall withstand the given limits without any irreversible damage.

Parameter	Min.	Max.	Unit	Note
Storage Temperature	-40	85	°C	
Storage Humidity (Relative)	-	85	%	no-condensing
Case Temperature	0	75	°C	
Operating Humidity (Relative)	-	85	%	no-condensing
Short term Operating Case Temperature		80	°C	<24 hours
Power Supply Absolute Range	-0.3	3.63	V	
RX Optical Maximum Input Power	-	10	dBm	

Operating Conditions

Parameter	Min.	Max.	Unit	Note
Operating Case Temperature	0	75	°C	
Operating Humidity (Relative)	-	85	%	no-Condensing
Power Supply Operating Range	3.135	3.465	V	
RX Optical Input Power	-	0	dBm	

Power Supply

The 400G ZR QSFP-DD DCO is a Power Class 8 module. In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted the module will proceed to High Power Mode without host intervention. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in below table. The power supply requirements are specified in the table below.

Parameter	Min.	Typ.	Max.	Unit	Note
3.3V DC Power Supply Voltage	3.135	3.3	3.465	V	
3.3V DC Power Supply Current			7	A	
Power Dissipation			18	W	
Low Power Consumption			1.5	W	
Module Inrush Current			100	mA/us	
Turn-off Current	-100			mA/us	
Power Supply Noise			25	mV	

High Speed Electrical Specifications

The transmitter and receiver comply with the CEI-56G-VSR-PAM4 electrical specification (OIF-CEI-04.0).

The data lines are AC-coupled and terminated in the module per the following figure from the QSFP-DD MSA. The high-speed signals follow the electrical specifications of CEI-56G-VSR-PAM as defined in OIF-CEI- 04.0.

The high speed signals consist of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n. These signals can be operated in 400GAUI-8 depending on the capability of the host. 400GAUI-8 mode provides 8 differential lanes using PAM4 signaling operating at 26.5625 GBaud. This results in 8 lanes of 50Gb/s for a total of 400Gb/s. This mode allows connection to PMD configurations of 400GUAI-8.

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Electrical Characteristics for Transmitter

Parameter	Min.	Typ.	Max.	Unit	Note
Signal Rate, each Lane		26.5625±100ppm		GBaud	
Differential Peak-Peak Input Voltage Tolerance			900	mVpp	

Electrical Characteristics for Receiver

Parameter	Min.	Typ.	Max.	Unit	Note
Signal Rate, each Lane		26.5625±100ppm			
Differential Peak-Peak Input Voltage Tolerance		750	900	mVpp	
Transition Time, 20% to 80%		9.5		ps	

Optical Transmitter

Parameter	Min.	Typ.	Max.	Unit	Note
Transmitter Frequency Range	191.3	193.7	196.1	THz	1
Laser Frequency Stability	-1.8		1.8	GHz	Frequency stability relative to ITU grid.
Laser Frequency Accuracy	-1.8		1.8	GHz	
Laser Frequency Fine Tuning Range	-6.0		6.0	GHz	
Fine Tuning Resolution		100		MHz	
Channel Tuning Speed	-		60	s	
Laser LineWidth			100	kHz	
Transmitter Output Power Range	-10		-6	dBm	
Transmitter Laser Disable Time			180	ms	
Output Power Stability	-0.5		0.5	dB	2
Output Power Accuracy	-2		2	dB	3
Transmitter Turn-up Time from Cold Start	-		120	s	
Transmitter OSNR (Inband)	34		-	dB/0.1nm	
Transmitter Back Reflectance	-		-24	dB	
Transmitter Output Power with TX Disabled	-		-20	dBm	

Parameter	Min.	Typ.	Max.	Unit	Note
Transmitter Polarization Dependent Power	-		1.5	dB	Power deference between X and Y polarization

Notes:

1. C band 75GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
2. Difference over temperature, time, wavelength and aging.
3. Difference between the set value and actual value over aging.

Optical Receiver

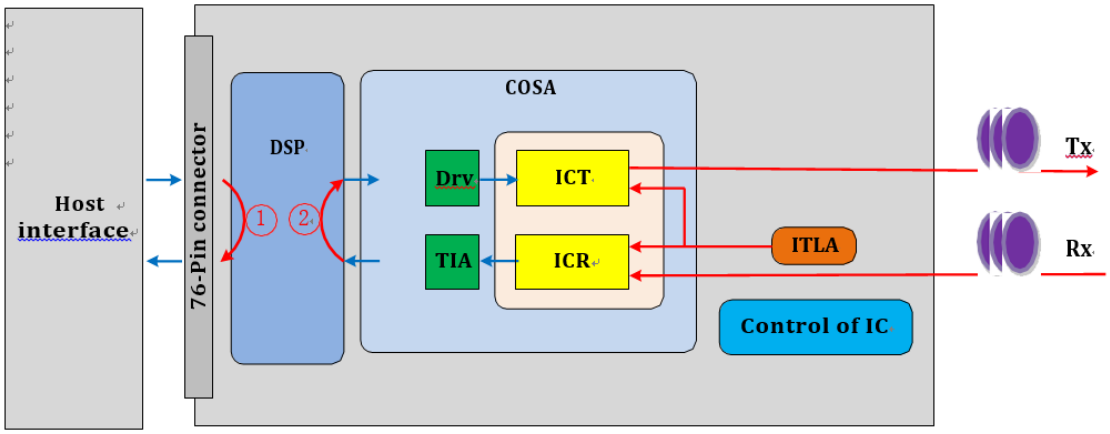
Parameter	Min.	Typ.	Max.	Unit	Note
Receiver Frequency Range	191.3	193.7	196.1	THz	
Input Power Range	-12		0	dBm	1
OSNR Sensitivity		24	26	dB/0.1nm	
Receiver Sensitivity			-20	dBm	2
Los Assert	-20		-16	dBm	
Los Hysteresis	1.0		2.5	dB	
CD Tolerance	2400			ps/nm	Tolerance to Chromatic Dispersion
PMD Tolerance	10			ps	3
Peak PDL Tolerance	3.5			dB	4
Tolerance to Change in SOP	50		-	rad/ms	
Input Power Transient Tolerance	-2		2	dB	5
Input Power Reading Accuracy	-2		2	dB	
Optical Return Loss	-20			dB	Optical reflectance at Rx connector input.
Receiver Turn-up Time from Cold Start	-		120	s	6

Notes:

1. Signal power of the channel at the OSNR Penalty < 0.5dB
2. Input power needed to achieve post FEC BER < 1E-15 when OSNR Tolerance > 26 dB/0.1nm
3. Tolerance to PMD with < 0.5 dB penalty to OSNR sensitivity.
4. Tolerance to peak PDL with < 1.3 dB penalty to OSNR sensitivity when change in SOP is < =1 rad/ms.
5. Tolerance to change in input power with <0.5 dB penalty to OSNR sensitivity.
6. From module reset, with valid optical input signal present.

Loopback

The module support loopback functionality. The host loopback (Loopback ①) and the network loopback (Loopback ②) are shown at bellowing figure. For details on controlling the loopback mode, please refer to Reference [2]. In optional loopback, TXn is looped back to RXn, for example TX0+ to RX0+, on both host and media side.



Insertion, Extraction and Retention Force

Parameter	Min.	Max.	Unit	Note
Insertion Force		90	N	
Extraction Force		50	N	
Retention Force	90		N	

EMI, EMC and ESD Specifications

The module is compliant with the requirements listed in the table below when installed in the host equipment.

Parameter	Reference	Value	Unit	Note
ESD Immunity	IEC 61000-4-2	8	kV	Contact Discharge
		15	kV	Air Discharge
ESD (HBM model)	JEDEC JESD22-A114-B	1	kV	High-Speed Contacts
		2	kV	Other pins
EMC Immunity	IEC 61000-4-3			
EMI Emission	FCC Class B			

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Don't directly look into the transmitter fiber connector at any time while the module is in operation.

Ordering Information

Product Name	Product Description
QDD-400G-ZR	QSFP DD 400G ZR PM-16QAM Plug-in, DWDM Tunable Coherent Transceiver, LC, DOM
JQDD-400G-ZR+HP	QSFP DD 400G OpenZR+ High Power Coherent JCO400-QDD-ZR-M-HP ZR+, Optical Transceiver, LC, DOM, Juniper Compatible

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