

400 Gb/s QSFP-DD DR4 500m Transceiver

QSFP-DD Series



- **Parallel 4 Optical Lanes**
- **Up to 500m transmission on single mode fiber (SMF) with FEC**
- **Maximum power consumption 12W**
- **8x53.125Gb/s electrical interface (400GAUI-8)**
- **Data Rate 106.25Gbps (PAM4) per channel**
- **IEEE802.3bs Specification compliant**
- **RoHS compliant**

Ascent's QSFP-DD-DR4-A05 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP- DD) optical module designed for 500m optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP- DD DR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an QSFP-DD MSA-compliant edge type connector.

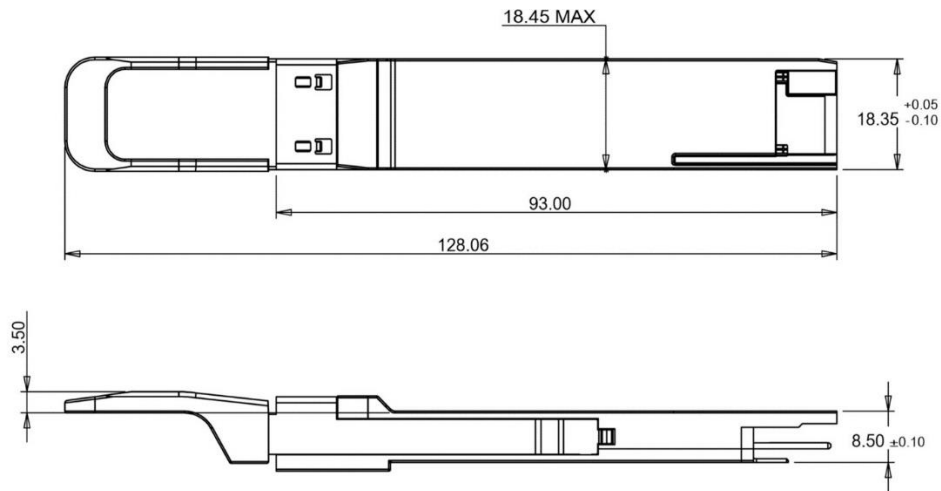
The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type.

It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

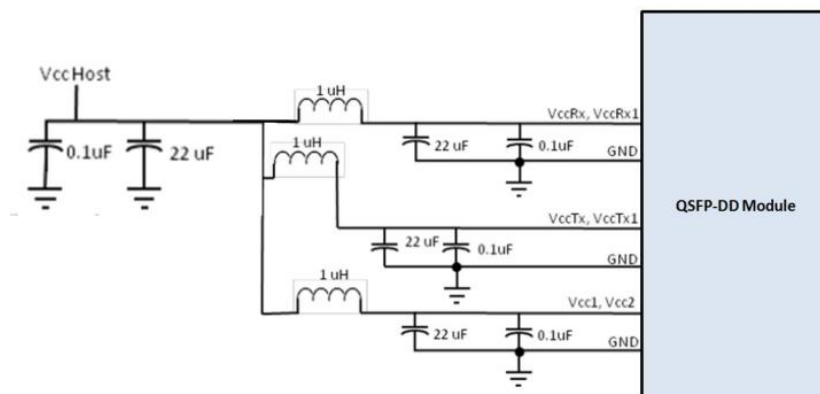
Key Features

- QSFP-DD MSA compliant
- Parallel 4 Optical Lanes
- IEEE802.3bs Specification compliant
- Up to 500m transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0 to 70°C
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel
- Maximum power consumption 12W
- MPO-12 connector
- RoHS compliant

Mechanical Dimensions

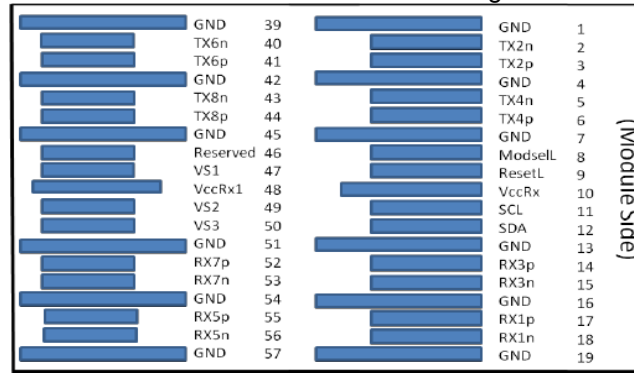


Recommended Power Supply Filter

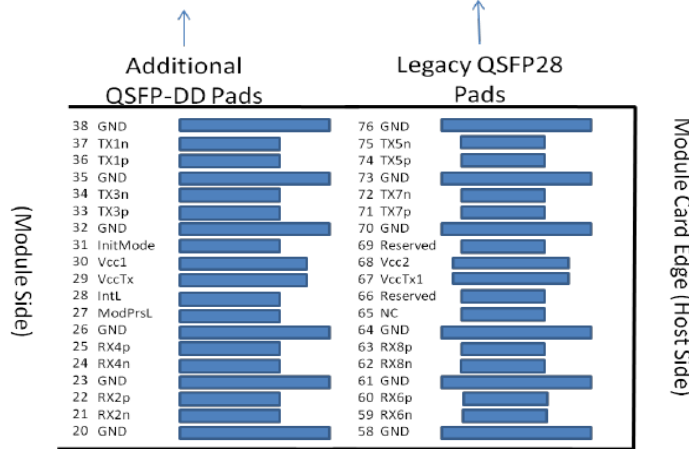


Pin Assignment

The electrical pinout of the QSFP-DD module is shown in the figure below.



Bottom side viewed from bottom



Top side viewed from top

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	2
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	3
4		GND	Ground	1B	4
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	5
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	6
7		GND	Ground	1B	7
8	LVTTL-I	ModSelL	Module Select	3B	8
9	LVTTL-I	ResetL	Module Reset	3B	9
10		VccRx	+3.3V Power Supply Receiver	2B	10
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	11
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	12
13		GND	Ground	1B	13
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	14
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	15
16		GND	Ground	1B	16
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	17
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	18

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
19		GND	Ground	1B	19
20		GND	Ground	1B	20
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	21
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	22
23		GND	Ground	1B	23
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	24
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	25
26		GND	Ground	1B	26
27	LVTTL-O	ModPrsL	Module Present	3B	27
28	LVTTL-O	IntL	Interrupt	3B	28
29		VccTx	+3.3V Power supply transmitter	2B	29
30		Vcc1	+3.3V Power supply	2B	30
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	31
32		GND	Ground	1B	32
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	33
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	34
35		GND	Ground	1B	35
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	36
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	37
38		GND	Ground	1B	38
39		GND	Ground	1A	39
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	40
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	41
42		GND	Ground	1A	42
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	43
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	44
45		GND	Ground	1A	45
46		Reserved	For future use	3A	46
47		VS1	Module Vendor Specific 1	3A	47
48		VccRx1	3.3V Power Supply	2A	48
49		VS2	Module Vendor Specific 2	3A	49
50		VS3	Module Vendor Specific 3	3A	50
51		GND	Ground	1A	51
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	52
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	53
54		GND	Ground	1A	54
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	55
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	56
57		GND	Ground	1A	57
58		GND	Ground	1A	58
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	59
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	60
61		GND	Ground	1A	61
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	62
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	63
64		GND	Ground	1A	64
65		NC	No Connect	3A	65
66		Reserved	For future use	3A	66

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
67		VccTx1	3.3V Power Supply	2A	67
68		Vcc2	3.3V Power Supply	2A	68
69		Reserved	For Future Use	3A	69
70		GND	Ground	1A	70
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	71
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	72
73		GND	Ground	1A	73
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	74
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	75
76		GND	Ground	1A	76

Specifications

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T _S	-40	85	°C	
Operating Case Temperature	T _{OP}	0	70	°C	
Power Supply Voltage	V _{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	T _{OP}	0		70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4x10 ⁻⁴		
Post-FEC Bit Error Ratio				1x10 ⁻¹³		1
Link Distance	D	0.5		500	km	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum transmission distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Consumption				12	W	
Supply Current	I _{CC}			3.64	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 GBd ± 100 ppm				
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

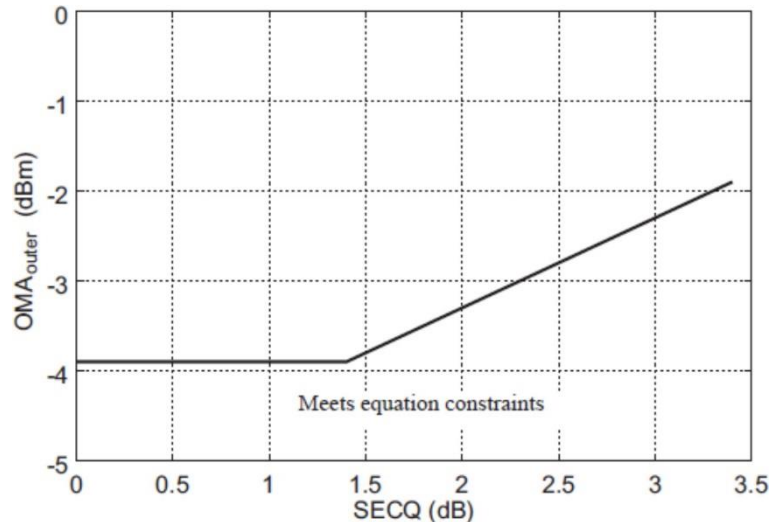
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Center Wavelength	λ_c	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30	1295.56		dB	Modulated
Average Launch Power, each Lane	P _{AVG}	-2.9	1300.05	4	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane	P _{OMA}	-0.8	1304.58	4.2	dBm	2
Launch Power in OMA _{outer} minus TDECQ, each Lane		-2.2	1309.14		dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	T _{DECC}			3.4	dB	
Extinction Ratio	ER	3.5			dB	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
RIN21.4OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			21.4	dB	
Transmitter Reflectance	TR			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P _{off}			-15	dBm	
Receiver						
Data Rate, each Lane		53.125			GBd	
		± 100				
		ppm				
Modulation Format		PAM4				
Damage Threshold, each Lane	THd	5			dBm	3
Average Receive Power, each Lane		-5.9		4	dBm	4
Receive Power (OMA _{outer}), each Lane				4.2	dBm	
Receiver Sensitivity (OMA _{outer}), each Lane	SEN			-4.4	dBm	5
Stressed Receiver Sensitivity (OMA _{outer}), each Lane	SRS			-1.9	dBm	6
Receiver Reflectance	RR			-26	dB	
LOS Assert	LOS _A	-30			dBm	
LOS De-assert	LOS _D			-12	dBm	
LOS Hysteresis	LOS _H	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
OMA _{outer} of each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
6. Measured with conformance test signal for BER = 2.4x10⁻⁴.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Digital Diagnostic Functions

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD-protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls, adjustments, or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Product Name

QSFP-DD-DR4-A05

Product Description

QSFP DD PAM4 Plug-in, 400GBASE-DR4 500m, 1310nm Optical Transceiver, MTP/MPO, DOM

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