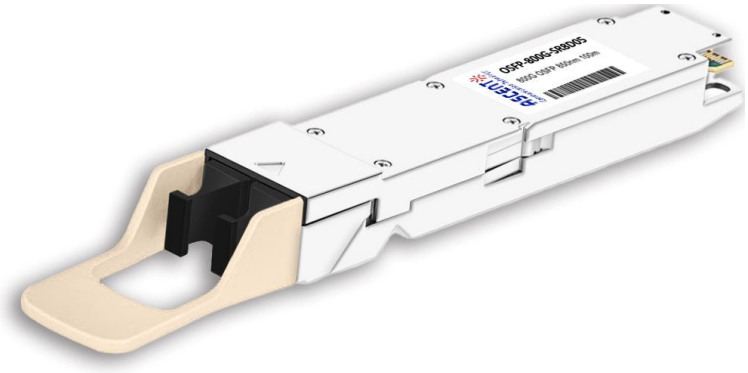
800 Gb/s OSFP SR8 50m Transceiver

OSFP Series



- **8x100G PAM4 retimed 800GAUI-8 electrical interface**
- **Maximum link length of 30m on OM3 or 50m on OM4**
- **Hot Pluggable OSFP form factor**
- **Compliant with CMIS 5.2**
- **Compliant with IEEE 802.3db**
- **Compliant to OSFP Module Specification Rev 5.0**

Ascent's OSFP-800G-SR8D-01 is an Eight-Channel, Parallel, Pluggable, Fiber-Optic OSFP for 800 Gigabit Ethernet applications. This transceiver is a high performance module for short-range data communication and interconnect application.

The 800GBASE-SR8 OSFP Optical Transceiver Module is designed for use in 800Gb/s systems throughput up to 30m over OM3 or 50m over OM4 multimode fiber (MMF) using a wavelength of 850nm via dual MTP/MPO-12 connectors.

Digital diagnostics functions are also available via the I2C interface, as specified by the OSFP MSA, to allow access to real time operating parameters. With these features, this easy to install, hot swappable transceiver is suitable to be used in various applications, such as data centers, high-performance computing networks, enterprise core and distribution layer applications.

Key Features

OSFP Serial Optical Interface:

- 8x100G PAM4 retimed 800GAUI-8 electrical interface
- Dual MPO- 12 APC connector is provided
- 8 channel VCSEL arrays and 8 channels PIN photo detector arrays
- Maximum link length of 30m on OM3 or 50m on OM4

OSFP MSA Compliant:

- Hot Pluggable OSFP form factor
- Compliant to OSFP Module Specification Rev 5.0
- Compliant with CMIS 5.2

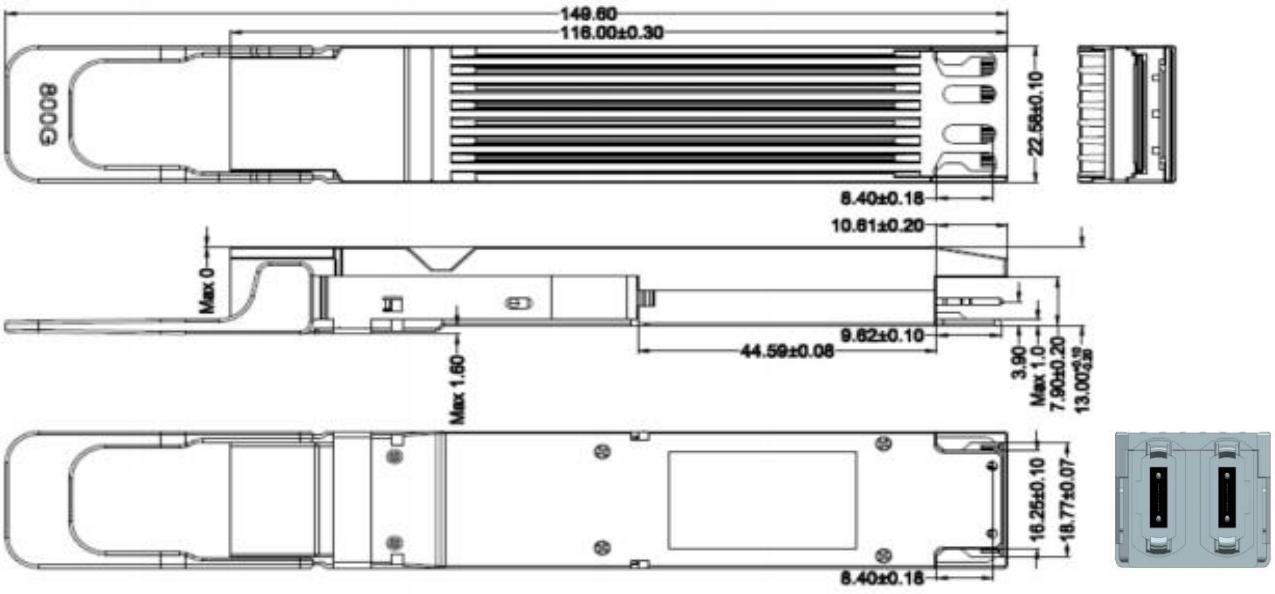
Support Protocol:

- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck

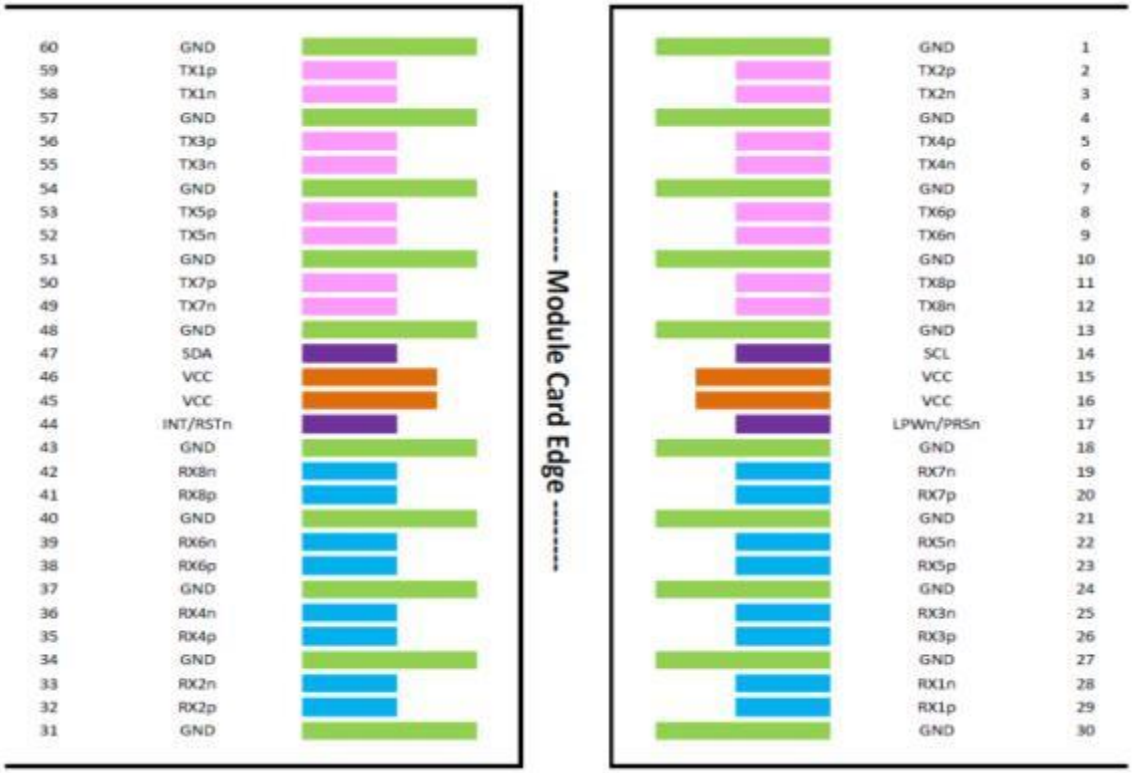
Low Power Consumption:

- Less than 14W in temperature range of 0 to 70°C

Mechanical Dimensions



Pin Assignment



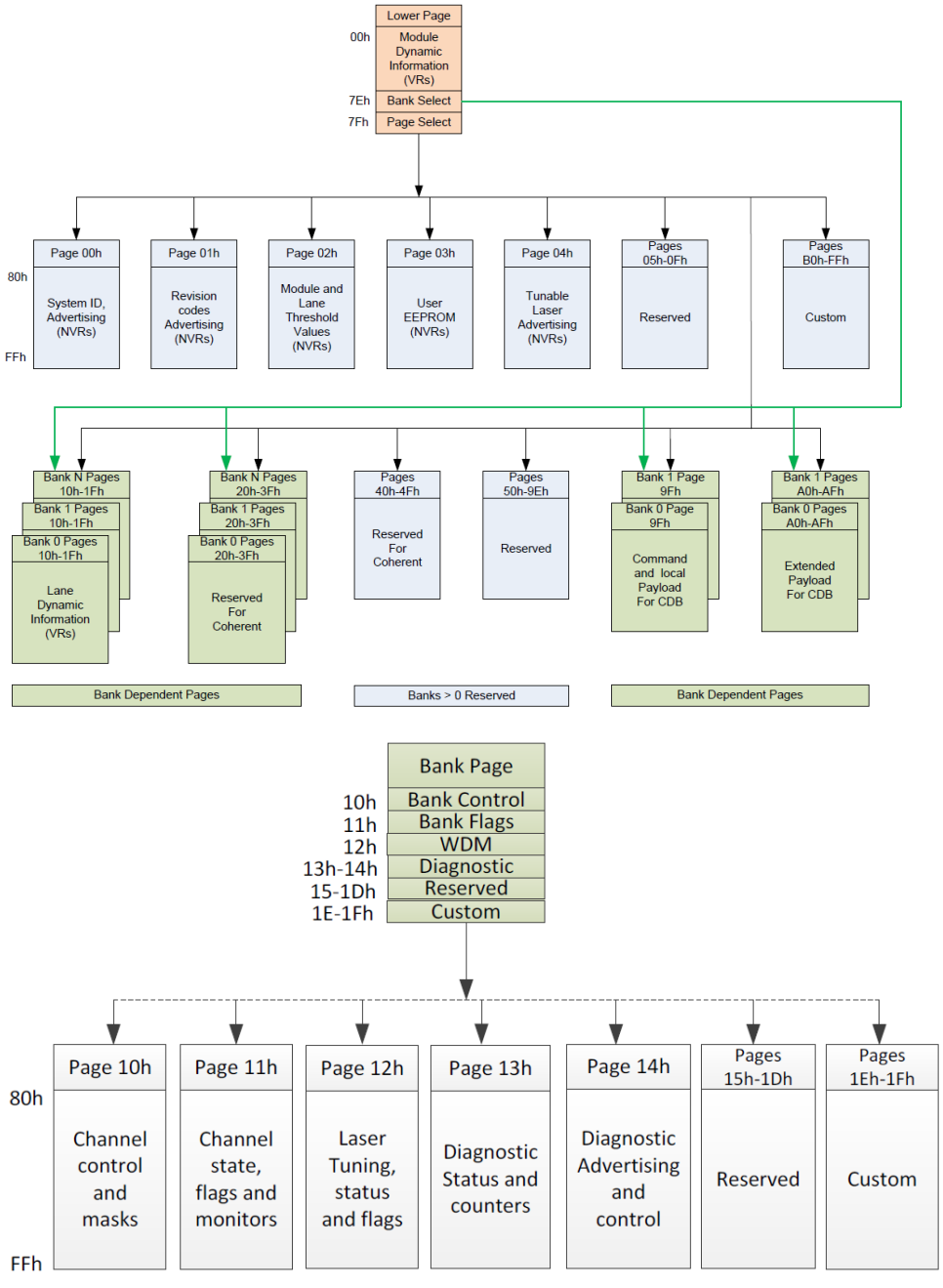
Pin #	Logic	Symbol	Description	Plug Sequence	Notes
1	GND		Ground	1	
2	Tx2p	CML-I	Receiver Data Non-Inverted	3	
3	Tx2n	CML-I	Receiver Data Inverted	3	
4	GND		Ground	1	
5	Tx4p	CML-I	Receiver Data Non-Inverted	3	
6	Tx4n	CML-I	Receiver Data Inverted	3	
7	GND		Ground	1	
8	Tx6p	CML-I	Receiver Data Non-Inverted	3	
9	Tx6n	CML-I	Receiver Data Inverted	3	
10	GND		Ground	1	
11	TX8p	CML-I	Receiver Data Non-Inverted	3	
12	TX8n	CML-I	Receiver Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS- I/O	2-wire Serial interface clock	3	
15	VCC		+3.3V Power	2	
16	VCC		+3.3V Power	2	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	3	1A
18	GND		Ground	1	
19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	
41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	3	1B
45	VCC		+3.3V Power	2	
46	VCC		+3.3V Power	2	
47	SDA	LVCMOS- I/O	2-wire Serial interface data	3	
48	GND		Ground	1	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	
59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

Notes:

1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.
2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3
3. INT/RSTnisa Multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2

Memory Map



Multiple Applications Support

The OSFP-800G-SR8D-01 supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Application Advertising

The OSFP-800G-SR8D-01 supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Address (Dec)	Application AppSel Code	Name	Value (Hex)	Description
86	0001b		HostInterfaceID	4B
87			MediaInterfaceID	D
88			HostLaneCount&MediaLaneCount	11
89			HostLaneAssignmentOptions	FF
01h:176			MediaLaneAssignmentOptions	FF
90	0010b		HostInterfaceID	11
91			MediaInterfaceID	10
92			HostLaneCount&MediaLaneCount	88
93			HostLaneAssignmentOptions	1
01h:177			MediaLaneAssignmentOptions	1
94	0011b		HostInterfaceID	E
95			MediaInterfaceID	0
96			HostLaneCount&MediaLaneCount	88
97			HostLaneAssignmentOptions	1
01h:178			MediaLaneAssignmentOptions	1
98	0100b		HostInterfaceID	51
99			MediaInterfaceID	12
100			HostLaneCount&MediaLaneCount	88
101			HostLaneAssignmentOptions	1
01h:179			MediaLaneAssignmentOptions	1
102	0101b		HostInterfaceID	4F
103			MediaInterfaceID	11
104			HostLaneCount&MediaLaneCount	44
105			HostLaneAssignmentOptions	11
01h:180			MediaLaneAssignmentOptions	11
106	0110b		HostInterfaceID	4D
107			MediaInterfaceID	1B
108			HostLaneCount&MediaLaneCount	22
109			HostLaneAssignmentOptions	55
01h:181			MediaLaneAssignmentOptions	55
110				FF
111				0
112				0
113				0
114				0
115				0
116				0
117				0

As shown in the table above, the OSFP-800G-SR8D supports 6 applications, 800GBASE-SR8, 400GBASE-SR8, 200GBASE-SR8, 2X400GBASE-SR4,4X200GBASE-SR2, and 8X100GBASE-SR1.

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0.
AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.
*Note that the channels of the module are independent and can be configured separately.
(ie. up to eight 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time.
OSFP-800G-SR8D-01 supports two methods of application selection and instantiation.
The first method is implemented according to CMIS, and the second method is customized, which is simpler.

First method

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation.
The Active Set can be read from page11h.
For example, select AppDescriptor3:
Step 1: Write 0x30 in Page10h Byte145~Byte152 (8 bytes)—Set AppselCode3
Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX Input Equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX Output Equalization

RX output Equalization follows CMIS Table below with default 1dB, readable and writable

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX Output Amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback Capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
13h:128	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Case Temperature	Top	0	70	°C	Operating Case Temperature
Relative Humidity(non-condensing)	RH	15	85	%	Relative Humidity(non-condensing)
Power Supply Voltage	Vcc	3.135	3.465	V	Power Supply Voltage
Total Power Consumption	Pc	-	14	W	Total Power Consumption
Supply Current per End			4.465	A	Supply Current per end
Bit Rate	BR		850	Gbps	Bit Rate
Fiber Length on OM3 MMF			30	m	Fiber Length on OM3 MMF
Fiber Length on OM4 MMF			50	m	Fiber Length on OM4 MMF
I2C Clock Frequency	0		400	kHz	I2C Clock Frequency

Notes:

1. Under condition of 3.465V operating supply voltage, and 70°C case temperature.

Optical Transmitter

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data Rate per Lane	DR		53.125		GBd	
Modulation Format		PAM4				
Center Wavelength 1	λ	840	860	868	nm	
RMS Spectral Width	σ			0.6	nm	
Average Launch Power, each lane	Pavg	-4.6		4	dBm	
Optical Power OMA, each Lane , max	P_{OMA}		3.5		dBm	
OMAouter, each Lane Min	P_{OMA}	max [-2.6 , max(TECQ,TECQ)– 4.4]			dBm	3
Transmitter and Dispersion Eye Closure (TDECQ), each Lane	TDECQ			4.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			4.4	dB	
Extinction Ratio	ER	2.5			dB	
Transmitter Power Excursion, each Lane				2.3	dBm	
Optical Return Loss Tolerance	ORLT			14	dB	
Optical Power for TX DISABLE				-30	dBm	

Parameter	Symbol	Min	Typ	Max	Unit
Encircled Fluxb2		≥86% at 19 um ≤30% at 4.5 um			

Notes:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4.
3. Max (TECQ, TDECQ) <1.8 dB and 1.8 < max (TECQ, TDECQ) < 4.4 dB

Optical Receiver

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Rate per Lane	BR		53.125		Gbd
Modulation Format		PAM4			
Center Wavelength	λ	842	850	948	nm
Damage Threshold		5			dBm
Average Receive Power, each Lane		–6.4		4	dBm
Receive Power, each Lane (OMAouter)				3.5	dBm
Receiver Reflectance	Rr			– 15	dB
Receiver Sensitivity, each Lane1		RS = max (-4.6 , TECQ - 6.4)			dBm
Stressed Receiver Sensitivity, each Lane				-2	dBm
Rx LOS	Assert	-15			dBm
	De-assert			-7.5	dBm
	Hysteresis	0.5		5	dB

Notes:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Electrical Specification

Parameter	Min.	Typ.	Max.	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential Pk-Pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye Height	10			mV
Common-Mode to Differential-Mode Return Loss	IEEE802.3ck Equation (120G-1)			dB
Vertical Eye Closure				dB
Effective Return Loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential Data Output Swing	300		900	mVpp
Differential Termination Mismatch			10	%
Eye Height	15			mV
Vertical Eye Closure			12	dB
Common-Mode to Differential-Mode Return Loss	IEEE802.3ck Equation (120G-1)			
Effective Return Loss	8.5			dB
Transition Time	8.5			ps

Laser Safety

The OSFP-800G-SR8D-01 are Class 1 Laser products according to FDA/CDRH, IEC-60825-1 and IEC60825-2 standards. They must be operated under the specified operating conditions

Electromagnetic Compatibility

The OSFP-800G-SR8D-01 are designed to meet FCC Class B limits.

Ordering Information

Product Name	Product Description
OSFP-800G-SR8D-01	OSFP 800GBASE-SR8 twin port transceiver, 800Gbps, 2xNDR, 2xMPO12 APC, 850nm MMF, up to 50m, finned

Contact Information

Ascent Communication Technology Ltd

AUSTRALIA
140 William Street, Melbourne
Victoria 3000, AUSTRALIA
Phone: +61-3-8691 2902

CHINA
Unit 1933, 600 Luban Road
200023, Shanghai, CHINA
Phone: +86-21-60232616

EUROPE
Pfarrer-Bensheimer-Strasse 7a
55129 Mainz, GERMANY
Phone: +49 (0) 6136 926 3246

Hong Kong SAR
Unit 9, 12th Floor, Wing Tuck Commercial Centre
177 Wing Lok Street, Sheung Wan, Hong Kong SAR
Phone: +852-2851 4722

USA
2710 Thomes Ave
Cheyenne, WY 82001, USA
Phone: + 1 203 350 9822

VIETNAM
11th Floor, Hoa Binh Office Tower
106 Hoang Quoc Viet Street, Nghia Do Ward
Cau Giay District, Hanoi 10649, VIETNAM
Phone: +84-24-37955917

WEB: www.ascentcomtec.com

EMAIL: sales@ascentcomtec.com

Ver. ACT_OSFP-800G-SR8D-01_Datasheet_V1d_Aug_2022