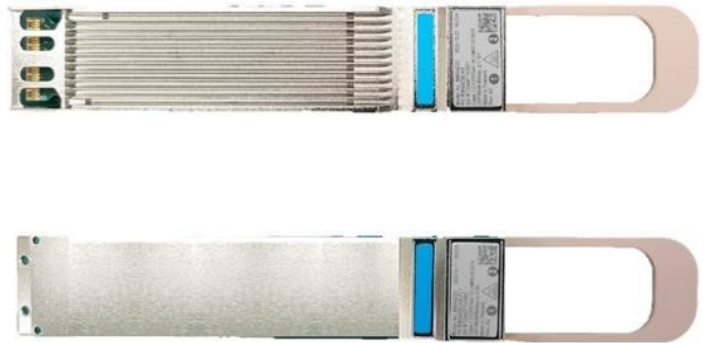


800 Gb/s SR8 OSFP 100 m Transceiver

OSFP Series

- OSFP form factor hot pluggable
- CMIS compliance
- 8 parallel lanes of 100G-PAM4 electrical and optical parallel lanes
- Dual optical port of MPO-12/APC
- Top open fin
- Up to 100m reach on multi-mode fiber OM4 and 50m on OM3 with FEC
- 14 Watts max
- Case temperature range of 0°C to 70°C



Ascent's OSFP-800G-SR8D-01 is 800 Gb/s Octal Small Form-factor Pluggable (OSFP) optical module with top open fin designed for 100 m with OM4 fiber optical communication applications. It is an InfiniBand and Ethernet 800Gb/s, 2x400Gb/s Twin-port OSFP, SR8 multimode, parallel, 8-channel transceiver using two, 4-channel MPO-12/APC optical connectors at 400Gb/s each.

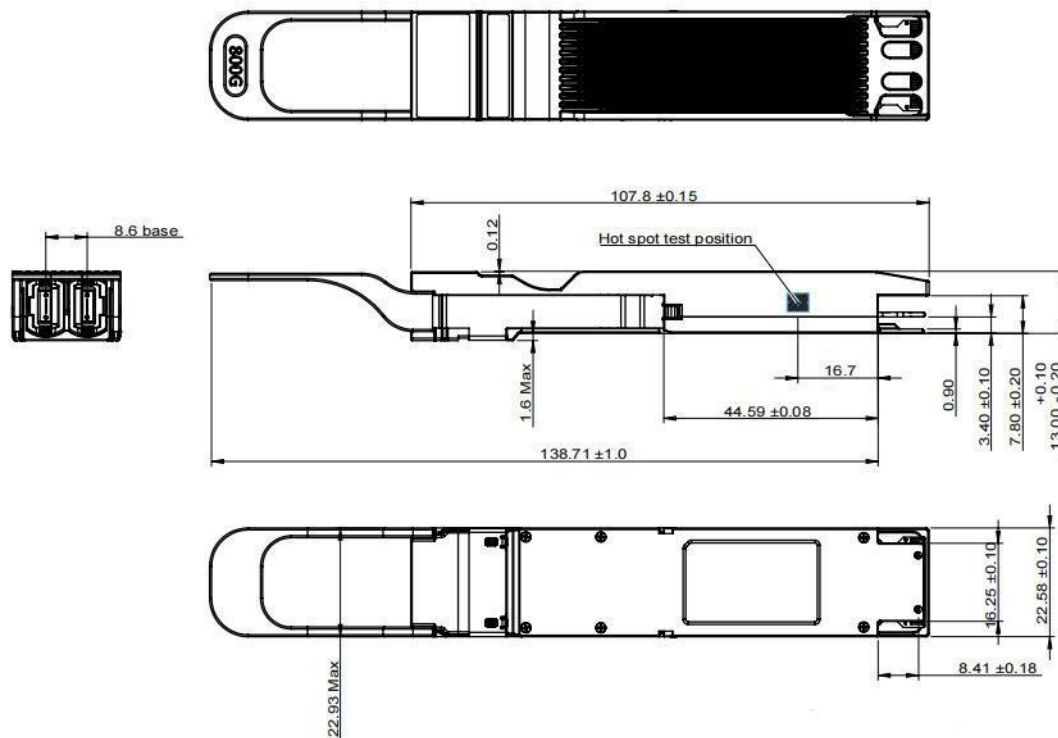
The module converts 8 channels of 100 Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100 Gb/s operation for an aggregate data rate of 800 Gb/s. Reversely, on the receiver side, the module converts 8 channels of parallel optical signals of 100 Gb/s each channel for an aggregate data rate of 800 Gb/s into 8 channels of 100 Gb/s (PAM4) electrical output data.

Dual MPO-12 connector can be plugged into the OSFP112 SR8 module receptacle for two sides with 4 channels each. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector. I2C interface is supported to read and control the status of this product. It is compatible with various NVIDIA Datacenter Switches.

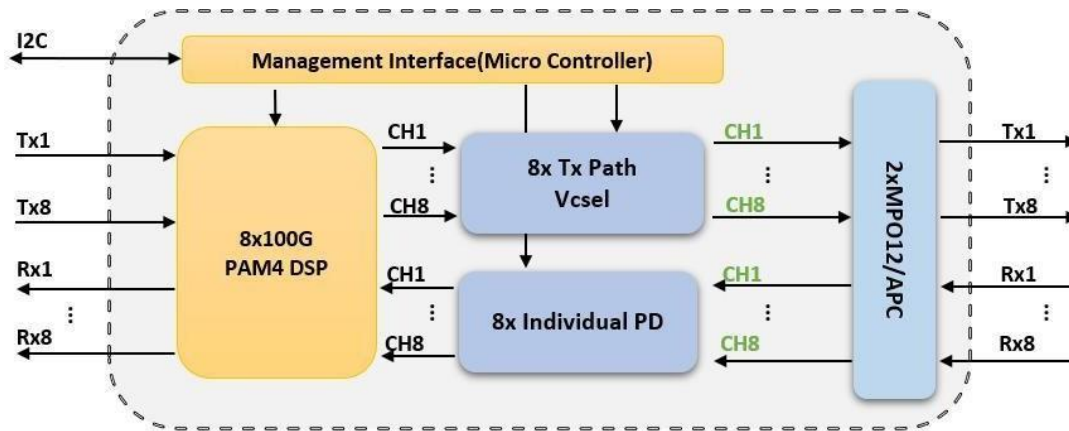
Key Features

- Compliant with common management interface specifications (CMIS)
- Adaptive Tx input equalization
- Programmable Rx output amplitude, Rx output pre-cursor, Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication, Tx fault indication
- Host and line side loopback capabilities, PRBS generator and checker capabilities
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

Mechanical Diagram



Transceiver Block Diagram

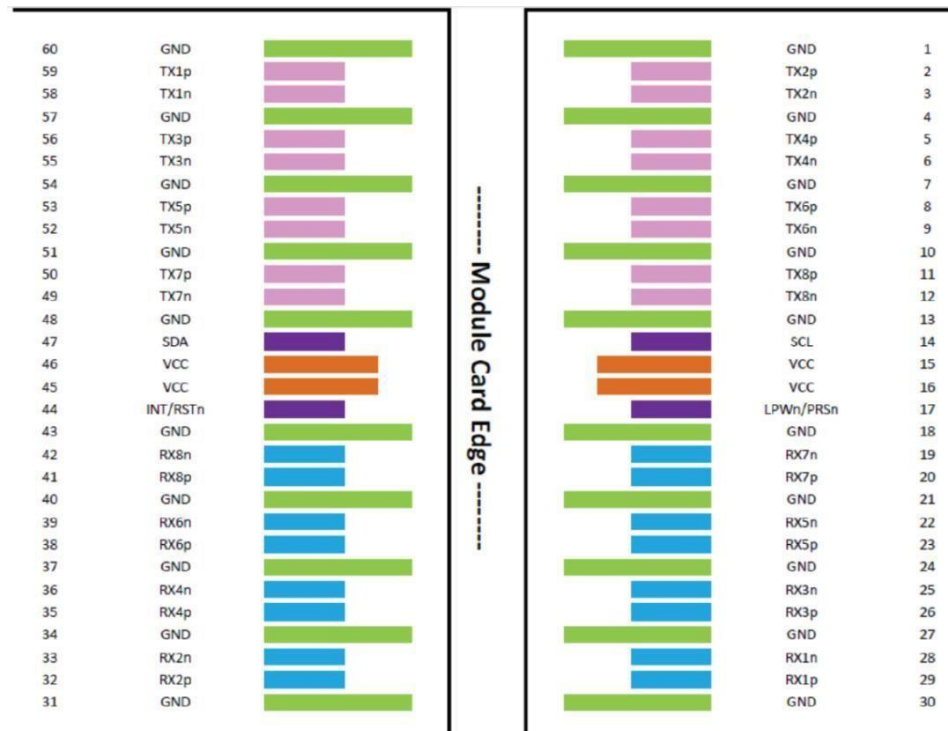


CMIS Application Advertisements

| ApSel Code | Host Electrical Interface | Module Media Interface | Host and Media Lane Count | Host Lane Assignment |
|------------|-----------------------------|------------------------|---------------------------|--|
| ApSel 1 | 50 (400GAUI-4-L C2M) | 11 (400GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) |
| ApSel 2 | 32 (IB NDR) | 11 (400GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) |
| ApSel 3 | F (200GAUI-4 C2M) | E (200GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) |
| ApSel 4 | 31 (IB HDR) | E (200GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) |
| ApSel 5 | 4C (100GAUI-1-L C2M) | D (100GBASE-SR) | 11 (1:1) | FF (lanes 1, 2, 3, 4, 5, 6, 7, 8) |
| ApSel 6 | 52 (800GAUI-8-L C2M) | 12 (800G-SR8) | 88 (8:8) | 01 (lane 1) |
| ApSel 7 | 4F (400GAUI-4-S C2M) | 11 (400GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) FF (lanes 1, 2, 3, 4, 5, 6, 7, 8) |
| ApSel 8 | 4B (100GAUI-1-S C2M) | D (100GBASE-SR) | 11 (1:1) | 3, 4, 5, 6, 7, 8) |
| ApSel 9 | 51 (800GAUI-8-S C2M) | 12 (800G-SR8) | 88 (8:8) | 01 (lane 1) |
| ApSel 10 | 42 (CAUI-4 C2M with RS FEC) | 9 (100GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) |
| ApSel 11 | 30 (IB EDR) | 9 (100GBASE-SR4) | 44 (4:4) | 11 (lanes 1, 5) |

Pin Assignment

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in the figure below, which is defined in Clause 8.1 of OSFP MSA Specification.



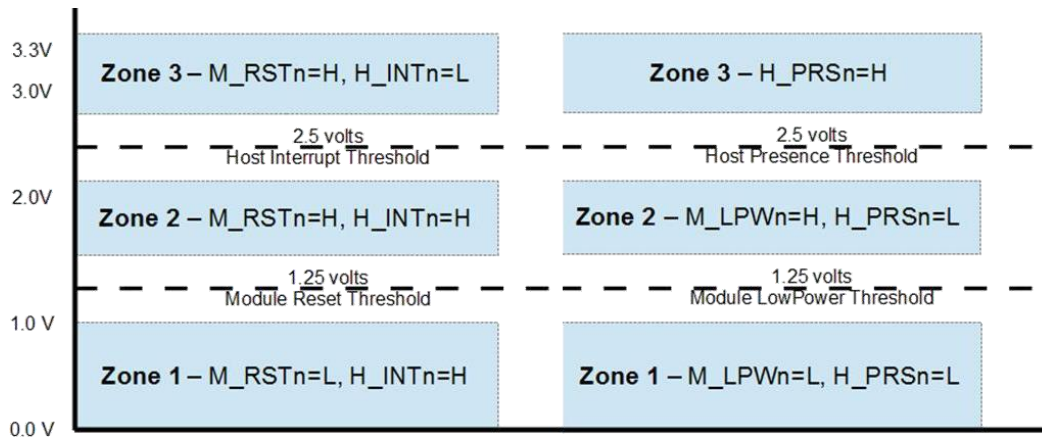
| Pin# | Symbol | Description | Logic | Direction | Plug Sequence |
|------|-----------|---------------------------------|-------------|-----------------|---------------|
| 1 | GND | | Ground | | 1 |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 4 | GND | | Ground | | 1 |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 7 | GND | | Ground | | 1 |
| 8 | TX6p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 10 | GND | | Ground | | 1 |
| 11 | TX8p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 12 | TX8n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 13 | GND | | Ground | | 1 |
| 14 | SCL | 2-wire Serial interface clock | LVC MOS-I/O | Bi-directional | 3 |
| 15 | VCC | +3.3V Power | | Power from Host | 2 |
| 16 | VCC | +3.3V Power | | Power from Host | 2 |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 |
| 18 | GND | | Ground | | 1 |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 |

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence |
|------|----------|---------------------------------|-------------|-----------------|---------------|
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 21 | GND | | Ground | | 1 |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 24 | GND | | Ground | | 1 |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 27 | GND | | Ground | | 1 |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 30 | GND | | Ground | | 1 |
| 31 | GND | | Ground | | 1 |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 34 | GND | | Ground | | 1 |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 37 | GND | | Ground | | 1 |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 40 | GND | | Ground | | 1 |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 43 | GND | | Ground | | 1 |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 |
| 45 | VCC | +3.3V Power | | Power from Host | 2 |
| 46 | VCC | +3.3V Power | | Power from Host | 2 |
| 47 | SDA | 2-wire Serial interface data | LVC MOS-I/O | Bi-directional | 3 |
| 48 | GND | | Ground | | 1 |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 51 | GND | | Ground | | 1 |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 53 | TX5p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 54 | GND | | Ground | | 1 |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 57 | GND | | Ground | | 1 |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 60 | GND | | Ground | | 1 |

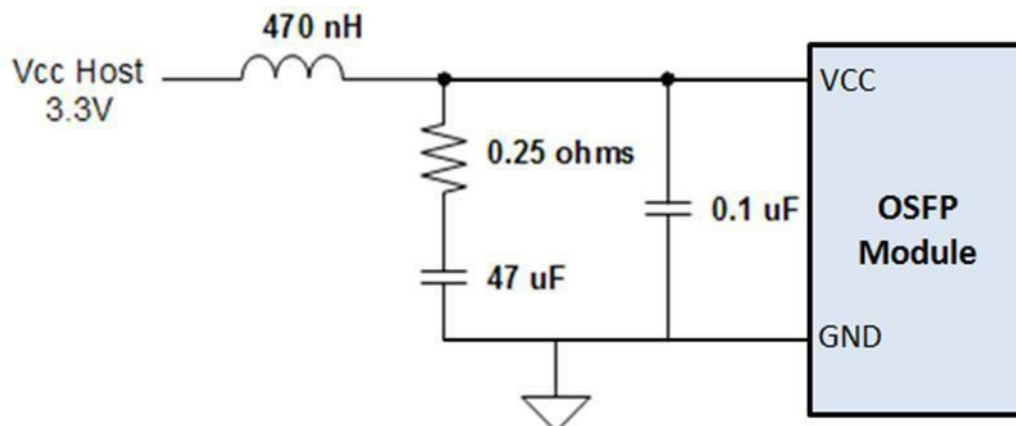
OSFP Control Pins

| Name | Direction | Description |
|-----------|--------------|--|
| SCL | BiDir | 2-wire serial clock signal. Requires pull-up resistor to 3.3V on host |
| SDA | BiDir | 2-wire serial data signal. Requires pull-up resistor to 3.3V on host. |
| LPWn/PRSn | Input/Output | Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3. |
| INT/RSTn | Input/Output | Dual Function Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3. |

Voltage Zones

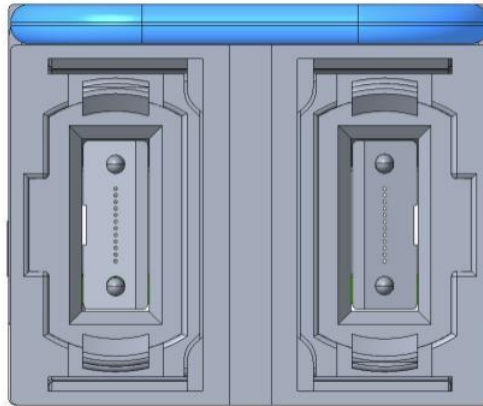


Recommended Power Supply Filter



Optical Port Description

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.



Optical Media Dependent Interface port assignments

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Specifications

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter | Symbol | Min. | Max. | Units | Note |
|----------------------------|-----------------|------|------|-------|----------------|
| Storage Temperature | T _S | -40 | 85 | °C | |
| Operating Case Temperature | T _{OP} | 0 | 70 | °C | |
| Power Supply Voltage | V _{CC} | -0.5 | 3.6 | V | |
| Relative Humidity | RH | 0 | 85 | % | Non-condensing |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|----------------------------|-----------------|-------|--------|----------------------|-------|------|
| Operating Case Temperature | T _{OP} | 0 | | 70 | °C | |
| Power Supply Voltage | V _{CC} | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 53.125 | | GBd | PAM4 |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | 2.4x10 ⁻⁴ | | |
| Post-FEC Bit Error Ratio | | | | 1x10 ⁻¹⁵ | | 1 |
| Link Distance (OM4) | D1 | 2 | | 100 | m | 2 |
| Link Distance (OM3) | D2 | 2 | | 50 | m | 2 |

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|---|-----------------|-----------------------------------|------|------|-------|------|
| Power Consumption | | | | 14 | W | |
| Supply Current | I _{CC} | | | 4.24 | A | |
| Module Input (each Lane) | | | | | | |
| Signaling Rate, each Lane | TP1 | 5325 ppm ± 100 ppm | | | GBd | |
| DC Common-Mode Input Voltage | TP1 | -0.35 | | 2.85 | V | |
| Single-Ended Input Voltage | TP1a | -0.4 | | 3.3 | V | |
| AC Common-Mode Voltage Tolerance | TP1a | | | | mV | |
| Low-Frequency, VCM _{LF} | | 32 | | | | |
| Full-Band, VCM _{LF} | | 80 | | | | |
| Module Stressed Input Tolerance | TP1a | IEEE 802.3ck D3.3 120G.3.4.3 | | | | |
| Differential Peak-to-Peak Input Voltage Tolerance | TP1a | 750 | | | mV | |
| Differential to Common-Mode Return Loss, RL _{cd} | TP1 | IEEE 802.3ck D3.3 Equation 120G-2 | | | dB | |

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|---|--------|------------------------------|------|------|-------|------|
| Effective Return Loss, ERL | TP1 | 8.5 | | | | |
| Differential Termination Mismatch | TP1 | | | 10 | | |
| Signaling Rate, Each Lane | TP4 | 53.125 ± 100 ppm | | | | |
| Peak-to-Peak AC Common-Mode Voltage | TP4 | | | | | |
| Low-Frequency, VCMLF | | | | 32 | | |
| Full-Band, VCMLF | | | | 80 | | |
| Differential Peak-To-Peak Output Voltage | TP4 | | | | mV | |
| Short Mode | | | | 600 | | |
| Long Mode | | | | 845 | | |
| Eye Height | TP4 | 15 | | | mV | |
| Vertical Eye Closure, VEC | TP4 | | | 12 | dB | |
| Common-Mode to Differential Return Loss, Rldc | TP4 | IEEE 802.3ck Equation 120G-1 | | | dB | |
| Effective Return Loss, ERL | TP4 | 8.5 | | | dB | |
| Differential Termination Mismatch | TP4 | | | 10 | % | |
| Transition Time | TP4 | 8.5 | | | ps | |
| DC Common-Mode Voltage Tolerance | TP4 | -0.35 | | 2.85 | V | |

Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|--|-------------|------------------------|------|------|-------|------|
| Transmitter | | | | | | |
| Data Rate, each Lane | | 53.125 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Center Wavelength | λ_c | 844 | 850 | 863 | nm | |
| RMA Spectral Width | | | | 0.6 | nm | |
| Average Launch Power, each Lane | P_{AVG} | -4.6 | | 4 | dBm | 1 |
| Outer Optical Modulation Amplitude (OMA_{outer}), each Lane | P_{OMA} | | | 3.5 | dBm | |
| For max(TECQ, TDECQ) ≤ 1.8 dB | | -2.6 | | | | |
| For 1.8 < max(TECQ, TDECQ) ≤ 4.4 dB | | -4.4+ max(TECQ, TDECQ) | | | | |
| Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane | TDECQ | | | 4.4 | dB | |
| Transmitter Eye Closure for PAM4, each Lane | TECQ | | | 4.4 | dB | |
| Overshoot/Undershoot | | | 29 | | % | |
| Transmitter Power Excursion | | | 2.3 | | dBm | |
| Extinction Ratio | ER | 2.5 | | | dB | |
| Transmitter Transition Time | Toff | | 17 | | ps | |
| Average Launch Power of OFF Transmitter | | | -30 | | dBm | |

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|--|--------|----------------------------------|------|---------------------|-------|------|
| RIN ₁₄ OMA | RIN | | | -132 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 14 | dB | |
| Encircled Flux | | ≥ 86% at 19μm ≤ 30% at 4.5 μm | | | dB | 2 |
| Receiver | | | | | | |
| Data Rate, each Lane | | 53.125 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Center Wavelength | λc | 842 | 850 | 948 | nm | |
| Damage Threshold, each Lane | THd | 5 | | | dBm | 3 |
| Average Receive Power, each Lane | | -6.4 | | 4 | dBm | 4 |
| Receive Power (OMA _{outer}), each Lane | | | | 3.5 | dBm | |
| Receiver Sensitivity (OMA _{outer}), each Lane | SEN | | | -4.6, TECQ - 6.4 | dBm | 5 |
| Stressed Receiver Sensitivity (OMA _{outer}), each Lane | SRS | | | -2.0 | dBm | 6 |
| Receiver Reflectance | RR | | -15 | | dB | |
| LOS Assert | LOSA | -15 | -8.6 | | dBm | |
| LOS De-assert | LOSD | | -6.6 | | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Conditions of Stress Receiver Sensitivity Test (Note 7) | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | | 4.4 | | dB | |
| OMA _{outer} of each Aggressor Lane | | | 3.5 | | dB | |

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4} .
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min. | Max. | Units | Notes |
|---|--------------|------|------|-------|----------------------------------|
| Temperature Monitor Absolute Error | DMI_Temp | -3 | 3 | °C | Over operating temperature range |
| Supply Voltage Monitor Absolute Error | DMI_VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX Power Monitor Absolute Error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias Current Monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX Power Monitor Absolute Error | DMI_TX_Ch | -2 | 2 | dB | 1 |

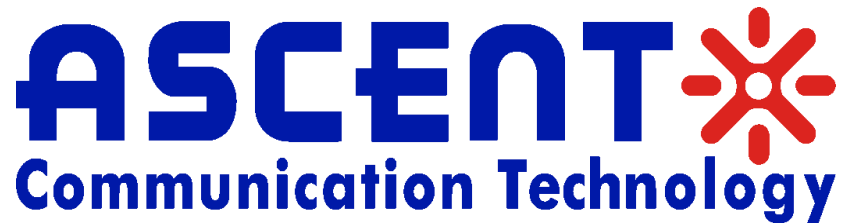
Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional ± 1 dB fluctuation, or a ± 3 dB total accuracy.

Ordering Information

| Product Name | Product Description |
|-------------------|---|
| OSFP-800G-SR8D-01 | OSFP-800G-SR8 NVIDIA twin port transceiver, 800 Gbps, 2xNDR, OSFP, 2xMPO12 APC, 850 nm MMF, up to 100 m, finned |

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