400 Gbps PSM8 Multi-Mode 100m OSFP Transceiver

400G OSFP Series

- OSFP MSA compliant
- 8 parallel lanes on 850nm center wavelength
- Compliant to IEEE 802.3bs specification
- Up to 100m transmission on Multi-Mode Fiber (MMF) OM3 with FEC
- Operating case temperature: 0°C
- to 70°C
- 8x53.125gb/s electrical interface (400GAUI-8)
- Data rate 53.125gbps (PAM4) per channel
- Maximum power consumption 12w
- MPO-16 connector
- RoHs compliant

Ascent's 400Gb/s Octal Small Form-factor Pluggable (OSFP) full-duplex optical module offers 8 independent transmit and receive channels, each capable of 53.125Gb/s operation for an aggregate data rate of 400Gb/s on 100 meters of OM3 multi-mode fiber.

An optical fiber cable with an MTP/MPO-16 connector can be plugged into the OSFP SR8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

The central wavelengths of all the 8 parallel lanes are 850nm. It contains an optical MPO-16 connector for the optical interface and a 60-pin connector for the electrical interface.

Host FEC is required to support up to 100m OM3 multi-mode fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the OSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Key Features

- OSFP MSA compliant
- 8 parallel lanes on 850nm center wavelength
- Compliant to IEEE 802.3bs Specification
- Up to 100m transmission on multi-mode fiber (MMF) OM3 with FEC
- Operating case temperature: 0°C to 70°C
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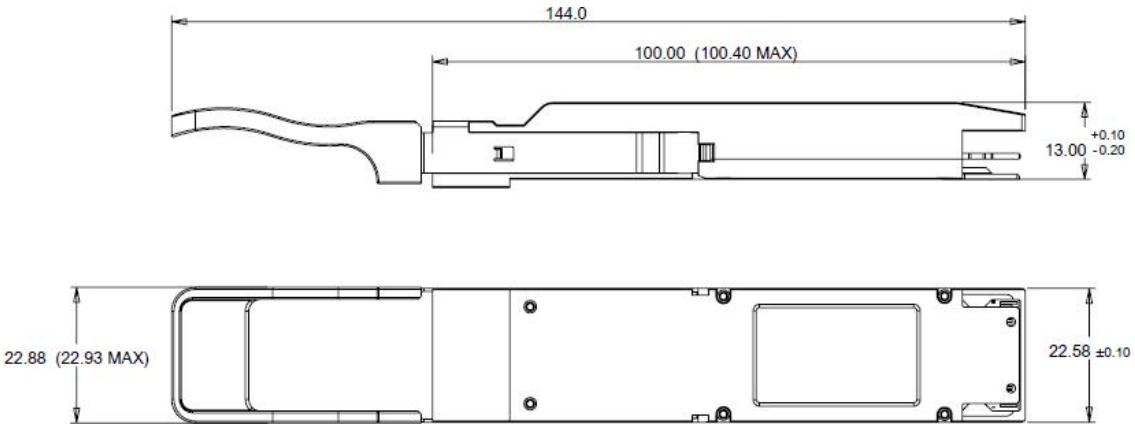
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 12W
- MPO-16 connector
- RoHS compliant

Mechanical Dimensions



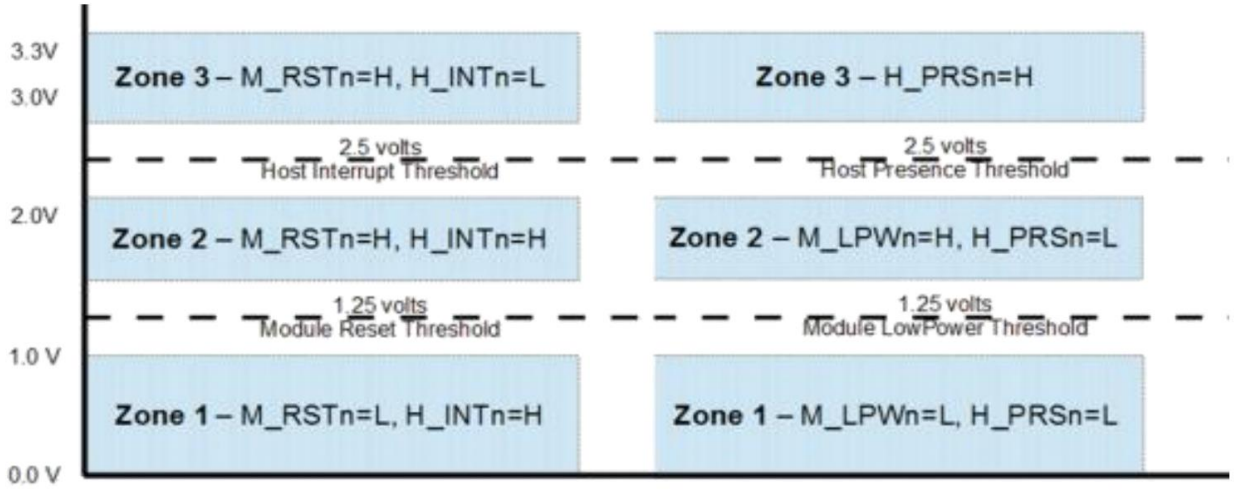
Functional Description

The module incorporates 8 parallel channels, on 850nm Center Wavelength, operating at50G per channel. The transmitter path incorporates an 8-channel CDR retimer, 2 sets of quad channel VCSEL drivers together with 2 sets of VCSEL arrays. On the receiver path,2 sets of photodiode arrays optics are coupled with an 8-channel CDR retimer. The electrical interface is compliant with IEEE 802.3bs and OSFP MSA in the transmitting and receiving directions, and the optical interface is compliant to OSFP MSA with MPO-16 Optical Connector. Figure 2 below shows the functional block diagram of this product.

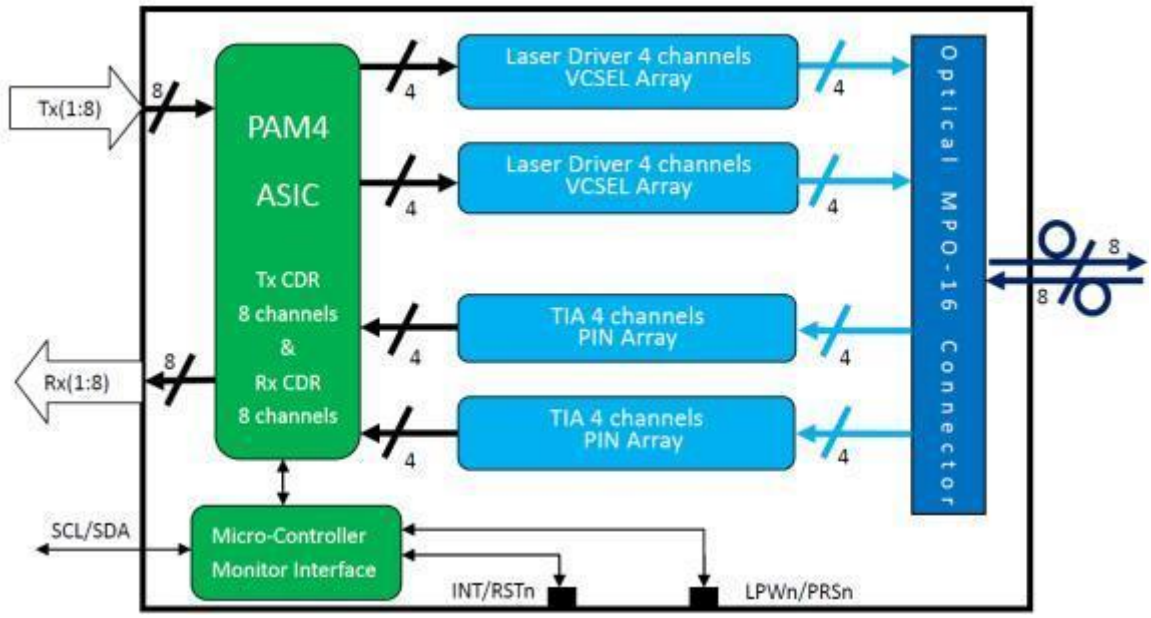
A single +3.3V power supply is required to power up this product. As per MSA specifications the module offers 4 low speed hardware control pins: SCL, SDA, INT/RSTnand LPWn/PRSn SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host.The pull-up resistor value can be 2.2kΩ to 4.7kΩ. NT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signalon the module which gets translated to an active-low signal on the host. The INT/

RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 1 shows these 3 zones. LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host. The LPWn

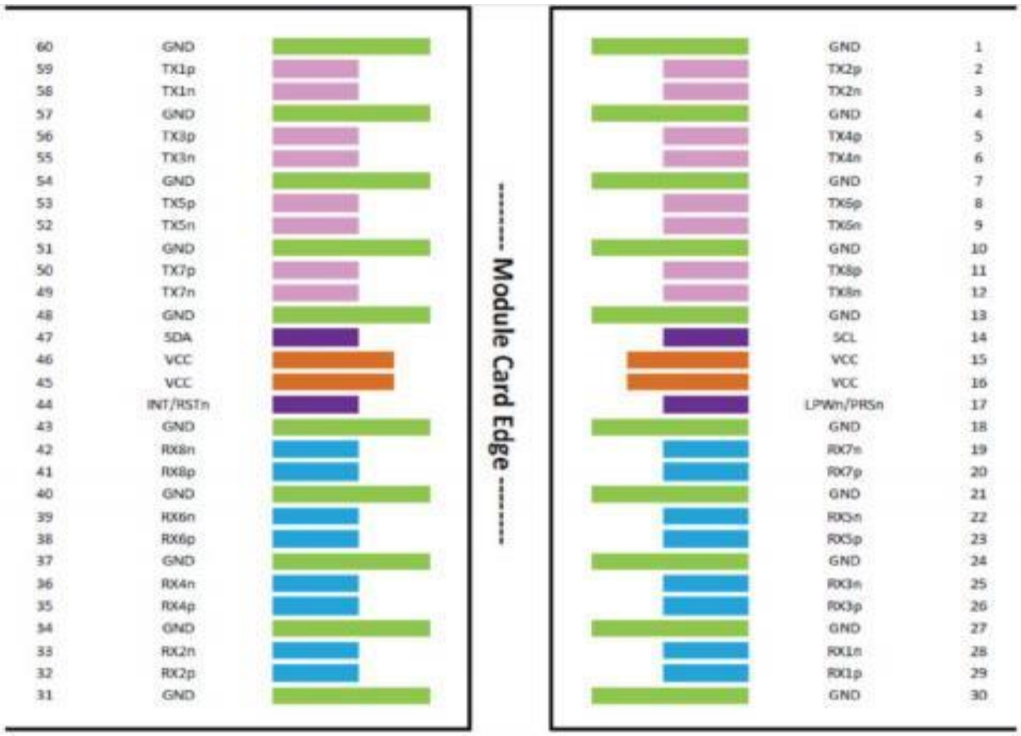
/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 1 shows these 3 zones.



Transceiver Block Diagram



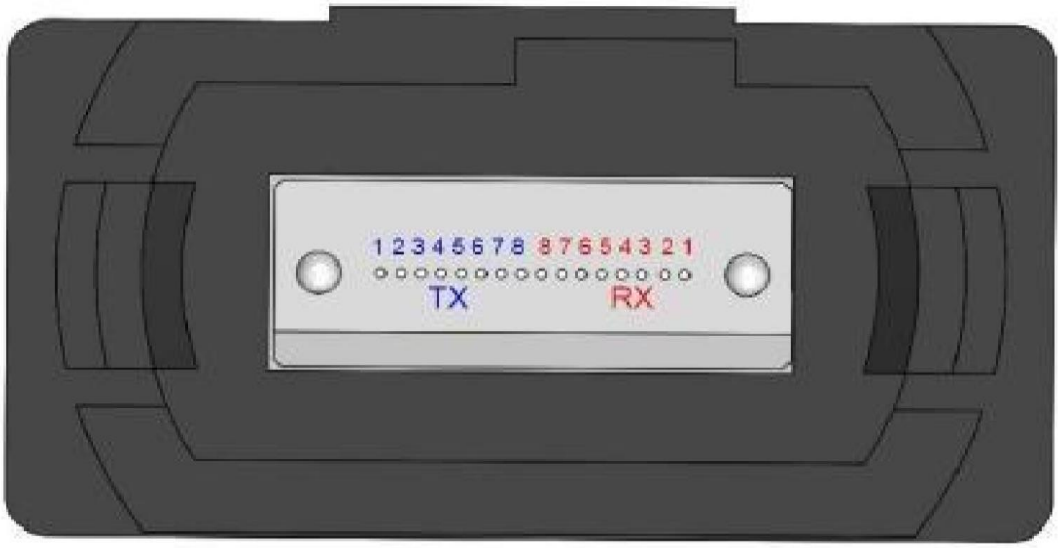
Pin Assignment and Description



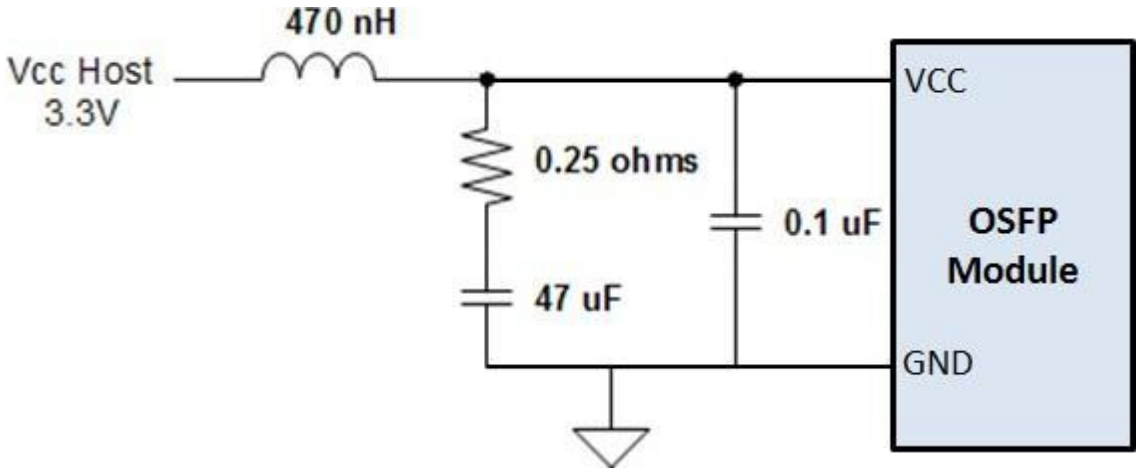
Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1



Recommended Power Supply Filter



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Power Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (non-condensation)	RH	0	85	%

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	0.5		100	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Consumption				12	W	
Supply Current	Icc			3.63	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	EEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	EEE 802.3-2015Equation (83E-6)			dB	
Module Stressed Input Tolerance	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-Ended Voltage Tolerance range(Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each Lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-End Eye Symmetry Mask Width (ESMW)	TP4		0.2 65		UI	
Near-End Eye Height, Differential	TP4	70			mV	
Far-End Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-End Eye Height, Differential	TP4	30			mV	
Far-End Pre-Cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Center Wavelength	λC	840	850	860	nm	
Data Rate, each Lane		26.5625± 100 ppm			GBd	
Modulation Format		PAM4				
RMS Spectral Width	Δλrms			0.6	nm	Modulated
Average Launch Power, each Lane	PAVG	-6.5		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	POMA	-4.5		3	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each Lan		-5.9			dB	
Transmitter and Dispersion Eye Clouser for PAM4, each Lane	TDECQ			4.5	dB	
Extinction Ratio	ER	3			dB	
Optical Return Loss Tolerance	TOL			12	dB	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Average Launch Power of OFF Transmitter, each Lane	Poff			-30	dBm	
Encircled flux		≥ 86% at 19 µm ≤ 30% at 4.5 µm				
Receiver						
Center wavelength	λ	840	850	860	nm	
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	THD	5			dBm	3
Average Receive Power, each Lane		-7.9		4	dBm	4
Receive Power (OMA_{outer}), each Lane				3	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			-6.5	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-3	dBm	6
Receiver Reflectance	RR			-12	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4		dB	
OMA_{outer} of each aggressor lane			3		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1 dB, the OMAouter (min) must exceed the minimum value specified here.

3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5. Receiver Sensitivity OMAouter, each lane (max) is informative and is defined for a BER of $2.4x10^{-4}$.

6. Measured with conformance test signal at receiver input for the BER of $2.4x10^{-4}$.

7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

Due to measurement accuracy of different single mode fibers, there could be an additional ±1 dB fluctuation, or a ±3 dB total accuracy.

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A(HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.d

Ordering Information

Product Name	Product Description
OSFP-400G-SR8-01	400G OSFP SR8 PAM4 850nm 100m DOM MTP/MPO-16 APC MMF Optical Transceiver Module

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