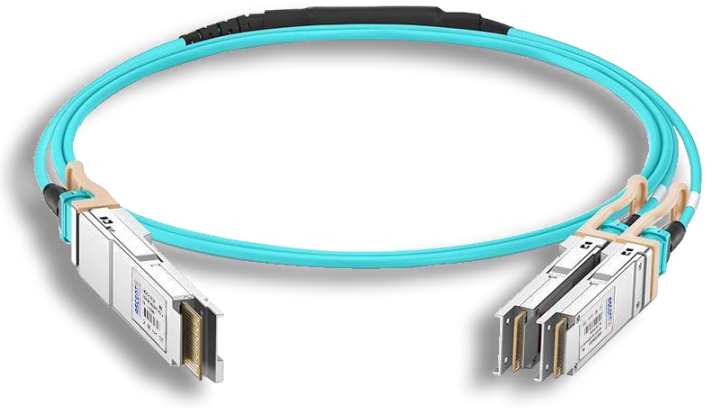
400G QSFP-DD to 2x 200G QSFP56 Active Optical Breakout Cable

QSFP-DD Cable Series



- **Enable 400G Breakout 2x200G Application**
- **Up to 53.125Gbps Data Rate Per Channel by PAM4 Modulation**
- **Support 400GAUI-8 Electrical Interface**
- **Integrated 850nm VCSEL Array and PD Array**
- **Low power consumption**
- **Hot Pluggable QSFP-DD and QSFP56 Form Factor**
- **Maximum Link Length: Up to 30m**

Ascent's 400G QSFP-DD to 2x200G QSFP56 breakout Active Optical Cable operates over Multi-Mode Fiber (MMF). It is designed for short-range data communication and interconnect applications.

The AOC has one QSFP-DD end connected to two QSFP56 ends. Each channel operates up to 53Gb/s and up to 100m using OM3 fiber.

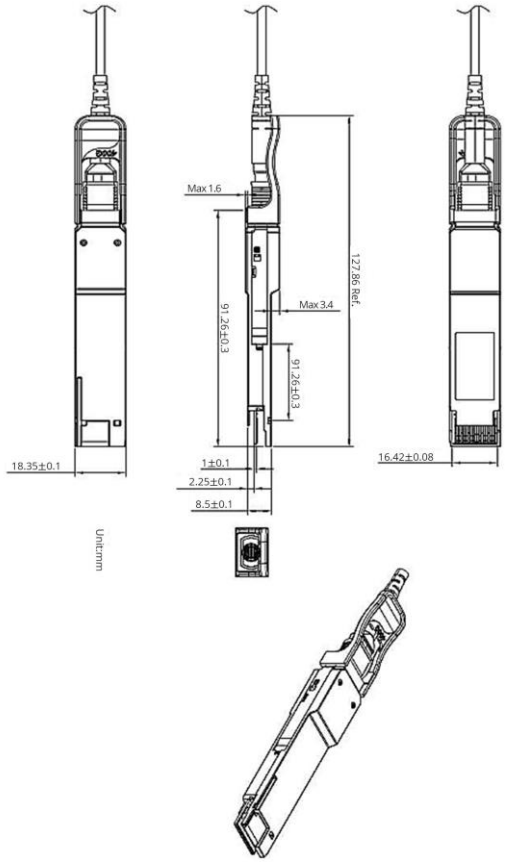
This breakout cable is compliant with IEEE 802.3, QSFP-DD MSA, SFF-8024, SFF-8679, SFF-8665, OIF-CEI-04.0 and CMIS 4.0. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

It provides connectivity between system units with a 400GbE connector on one side and two separate 200GbE connectors on the other side and is suitable for Data Center Applications.

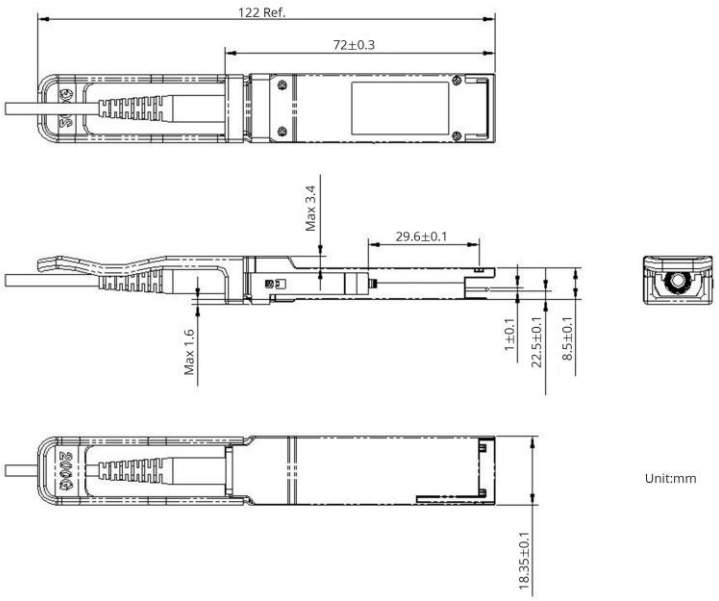
Key Features

- IEEE 802.3cd, IEEE 802.3bs Annex120E
- OIF-CEI-04.0
- QSFP-DD MSA, QSFP-DD-CMIS-Rev4.0
- SFF-8024 Rev. 4.6, SFF-8679 Rev1.8, SFF-8665 Rev1.9
- Up to 53.125Gbps Data Rate Per Channel by PAM4 Modulation
- Enable 400G Breakout 2x200G Application
- Support 400GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- Power Dissipation: <5W (200G End) , <11W (400G End)
- Hot Pluggable QSFP-DD and QSFP56 Form Factor
- Maximum Link Length: Up to 30m
- Operating Case Temperature Range: 0 to +70°C
- EEPROM in Cable Assembly
- Pre-FEC Max. BER 2.4E-4
- Support RS-FEC
- Single 3.3V Power Supply
- DDM Function Implemented

Diagram Mechanical Drawing

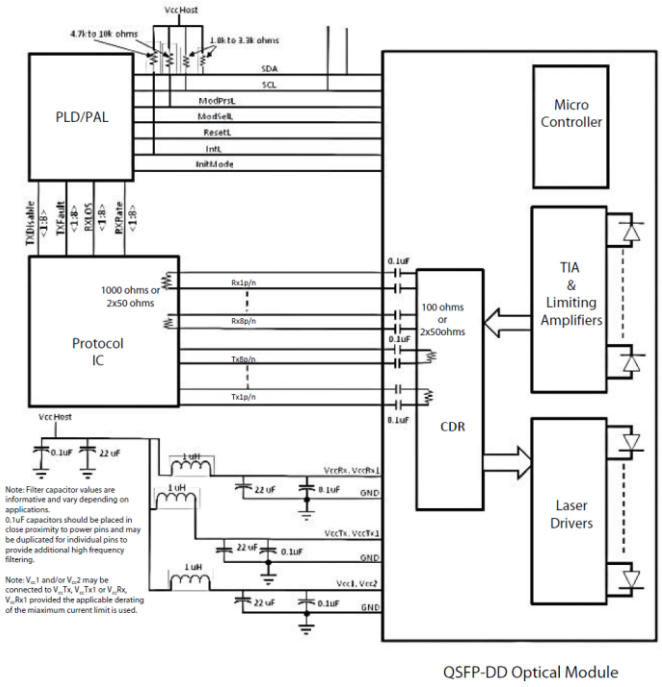


QSFP-DD Diagram Mechanical Drawing

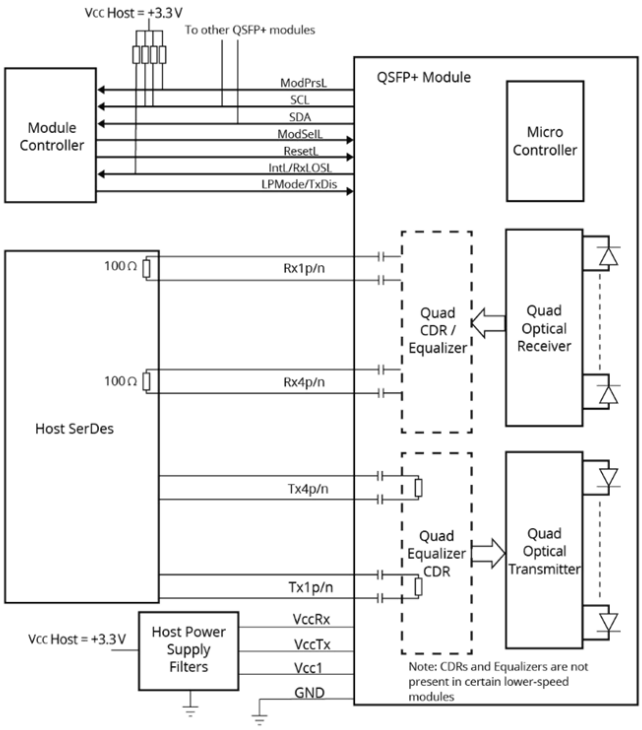


QSFP56 Diagram Mechanical Drawing

Principle Diagram

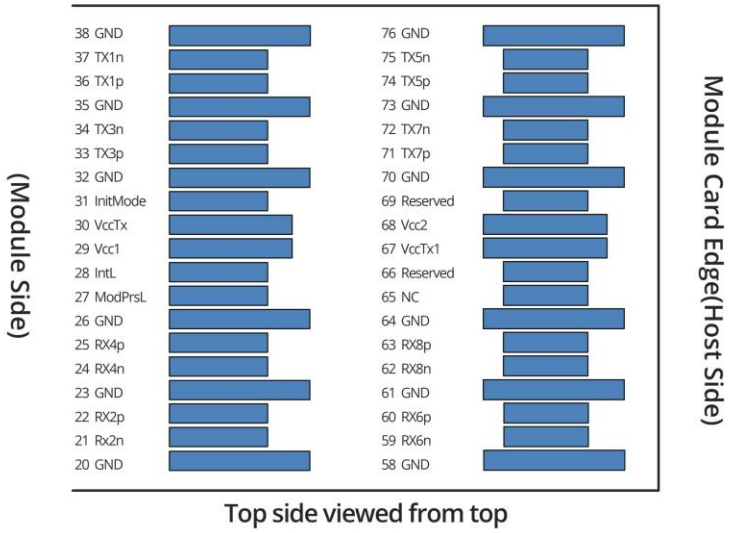


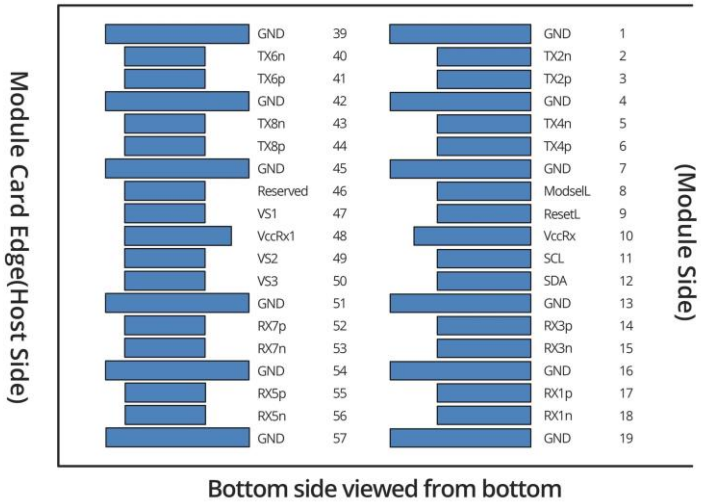
QSFP-DD Principle Diagram



QSFP56 Principle Diagram

QSFP-DD Pin Assignment





Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7				1
		GND	Ground	
8	LVTTL-I	ModSelL	Module Select	
Pin	Logic	Symbol	Description	Note
9	LVTTL-I	ResetL	Module Reset	

10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	
				1
17	CML-O	GND	Ground	
18	CML-O	Rx1p	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VCCTx	+3.3 V Power Supply Transmitter	2
30		VCC 1	+3.3 V Power Supply	2
31	LVTTL-I	InitMode	Initialization Mode; In Legacy QSFP Applications, the IntiMode Pad Is Called LPMode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	
45		GND	Ground	1
46		Reserved	For Future Use	3
47		VS1	Module Vendor Specific 1	3
48		VCCRxx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1

59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For Future Use	3
67		VCCTx 1	+3.3 V Power Supply Transmitter	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Inverted Data Input	
72	CML-I	Tx7n	Transmitter Non-Inverted Data Output	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	
75	CML-I	Tx5n	Transmitter Non-Inverted Data Output	
76		GND	Ground	1

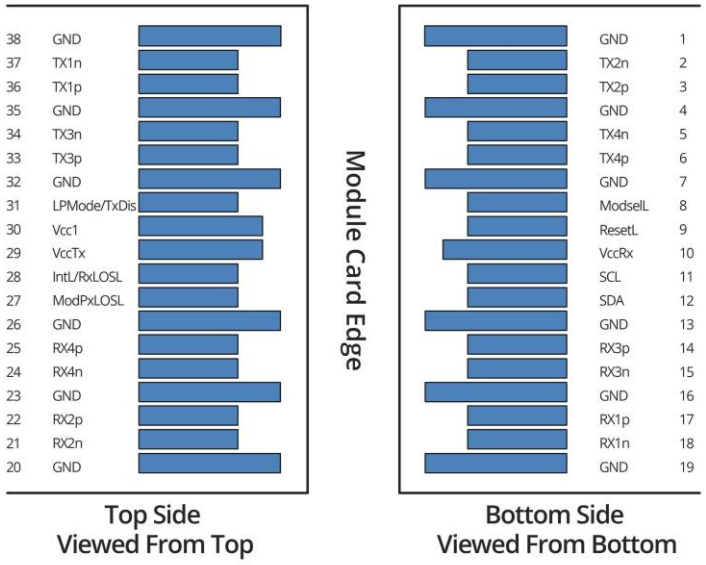
Notes

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected theses directly to the host board signal common ground plane.

2. V_{CC}Rx, V_{CC}Rx1, V_{CC}1, V_{CC}2, V_{CC}Tx, and V_{CC}Tx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in the table above. V_{CC}Rx, V_{CC}Rx1, V_{CC}1, V_{CC}2, V_{CC}Tx, and VCCTx1 may be internally connected within the module in any combination. The connector V_{CC} pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 Ω to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kΩ and less than 100 pF.

QSFP56 Pin Assignment



Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		V_{CC} Rx	+3.3V Power Supply for Receiver	2
11	LVTTL-I/O	SCL	2-wire Serial Interface Clock	
12	LVTTL-I/O	SDA	2-wire Serial Interface Data Line	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Interted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1

27	LVTTL-O	ModPrsL	Module Present		
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally Configurable as RxLOSL via the Management Interface (SFF-8636)		
29		V_{CC}Tx	+3.3V Power Supply for Transmitter		
Pin	**Logic**	**Symbol**	**Description**	**Plug Sequence**	**Note**
30		V_{CC}1	+3.3v Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode. Optionally Configurable As TxDis Via the Management Interface (SFF-8636)	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	T_S	-20	85	°C
Supply Voltage	V_{CC}	-0.5	4.0	V
Operating Relative Humidity	RH	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Bit Rate (per Channel)	BR		26.5625		GBd
Humidity	RH	5		85	%
Fiber Bend Radius	RB	3			cm

Electrical Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Note
Supply Voltage	V_{CC}					
	V_{CC}3.3Tx	V	3.135	3.3	3.465	
	V_{CC}3.3-Rx					
Power Consumption (QSFP-DD)	Pc	W		11		Per-end
Power Consumption (QSFP56)	Pc	W		5		Per-end
Transceiver Power-On Initialize Time		ms			2000	

Transmitter					
Differential Peak-to-Peak Input Voltage Tolerance		mV	900		
Differential Termination Mismatch					10%
Differential Input Return Loss (SDD11)		dB			See CEI-56G-VSR
Common-Mode to Differential Conversion and Differential to Common-Mode Conversion (SCD11, SDC11)		dB			See CEI-56G-VSR
Receiver					
Differential Peak-to-Peak Output Voltage		mV			900
DC Common Mode Voltage	Vcm	mV	-350		2850
AC Common Mode Noise, RMS		mV			17.5
Differential Termination Mismatch		%			10
Differential Output Return Loss (SDD22)		dB			See CEI-56G-VSR
Common-mode to Differential Conversion and Differential to Common-mode Conversion (SCD22, SDC22)		dB			See CEI-56G-VSR
IIC Communication					
IIC Clock Frequency (QSFP-DD)		kHz		400	1000
IIC Clock Frequency (QSFP56)		kHz		100	1000
Clock Stretching		µs			500

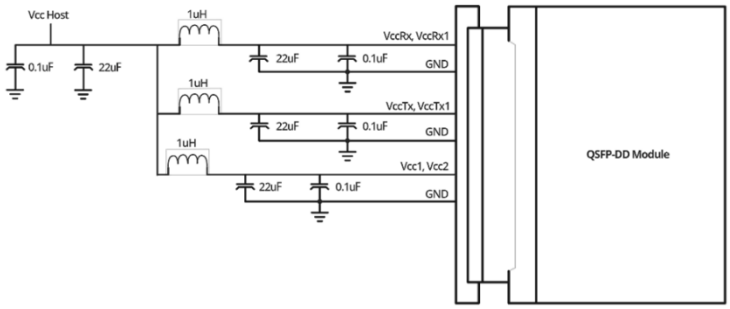
Module Memory Map

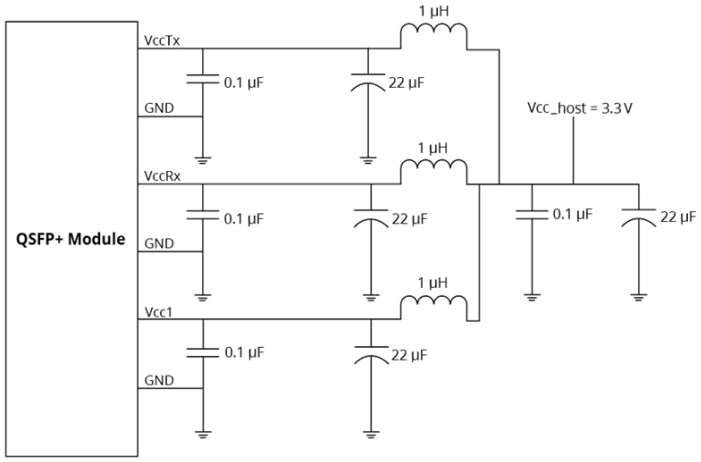
Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

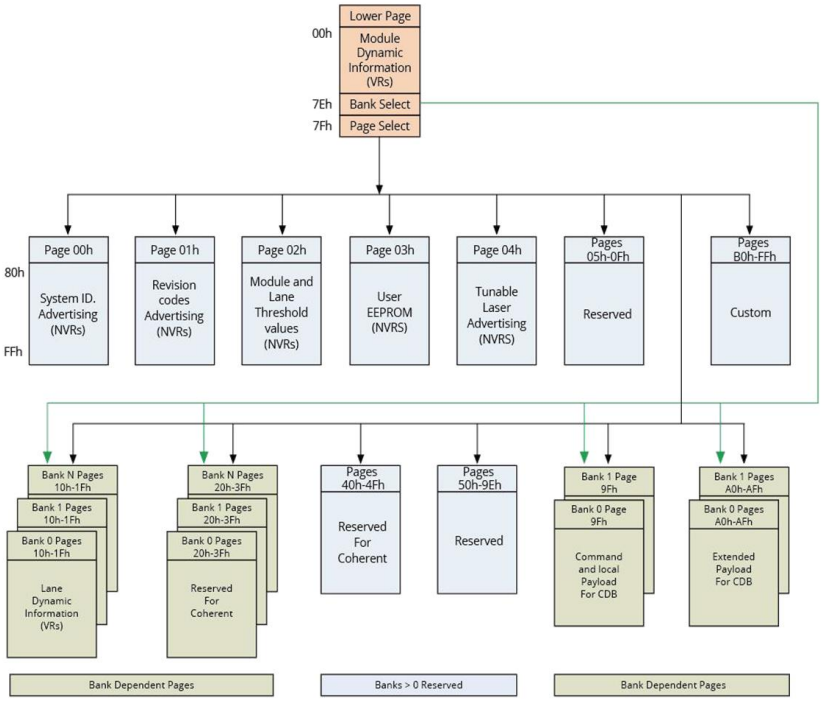
Note: Filter capacitor values are informative and vary depending on applications.

Note: Vcc1 and/or Vcc2 may be connected to V_{CC}Tx, V_{CC}Tx1 or V_{CC}Rx, V_{CC}Rx1 provided the applicable derating of the maximum current limit is used.





QSFP-DD Recommended Host Board Power Supply Filtering



QSFP56 Recommended Host Board Power Supply Filtering

Ordering Information

Product Name	Product Description
QDD4-2B1-AOC-003	400G QSFP-DD to 2x200G QSFP56 Active Optical Breakout Cable, IB twin port HDR, 3m
QDD4-2B1-AOC-005	400G QSFP-DD to 2x200G QSFP56 Active Optical Breakout Cable, IB twin port HDR, 5m
QDD4-2B1-AOC-010	400G QSFP-DD to 2x200G QSFP56 Active Optical Breakout Cable, IB twin port HDR, 10m
QDD4-2B1-AOC-015	400G QSFP-DD to 2x200G QSFP56 Active Optical Breakout Cable, IB twin port HDR, 15m
QDD4-2B1-AOC-030	400G QSFP-DD to 2x200G QSFP56 Active Optical Breakout Cable, IB twin port HDR, 30m

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